Optimizing for Size: Exploring the Limits of Code Density

Vincent M. Weaver
Cornell University

ASPLOS XIV Poster Session, 8 March 2009

Sally A. McKee
Chalmers University of Technology

Abstract

Reductions in instruction count can improve cache and bandwidth utilization, lower power consumption, and increase overall performance. Nonetheless, code density is often overlooked when studying processor architectures.

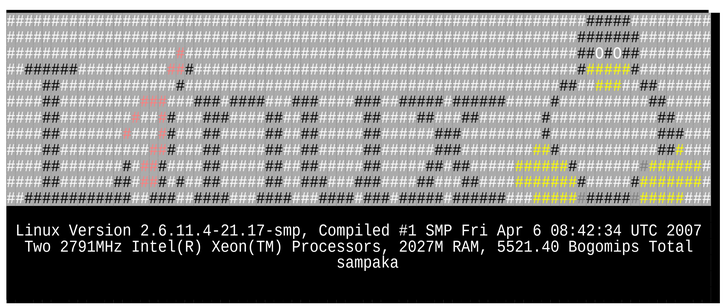
We hand-optimize an embedded benchmark for size in assembly language on 20 different instruction set architectures and investigate the architectural features that contribute most heavily to code density.

Background

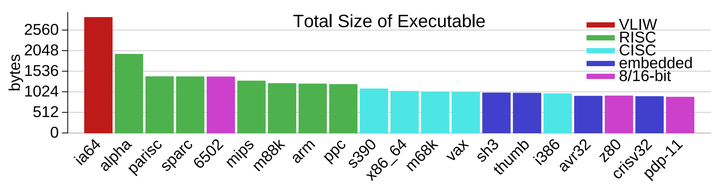
The 20 architectures investigated can be broadly broken into 5 categories:

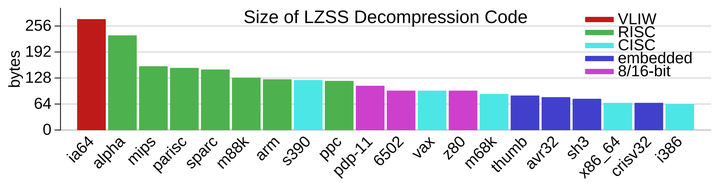
Type	Represented Architectures	Instr Length (bytes)	Opcode Args
VLIW	ia64	16/3	3
RISC	alpha, arm, m88k, mips pa-risc, ppc, sparc	4	3
CISC	m68k, s390, vax, x86, x86_64	1-54	2
Embedded	avr32, crisv32, sh3, THUMB	2	2
8/16-bit	6502, pdp-11, z80	1-6	1-2

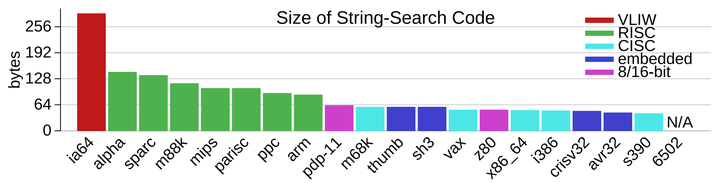
Below is the output from the benchmark tool. It uses LZSS decompression, file I/O, and string manipulation.

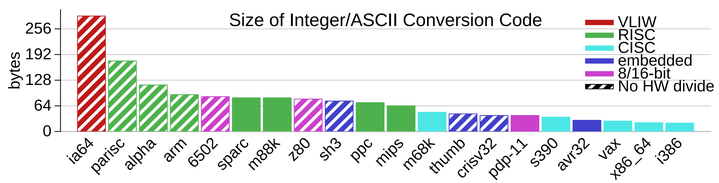


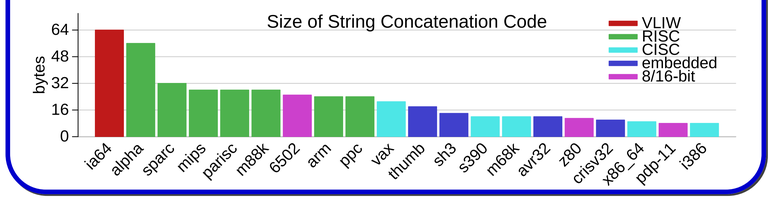
Hand-Optimized Assembly Results









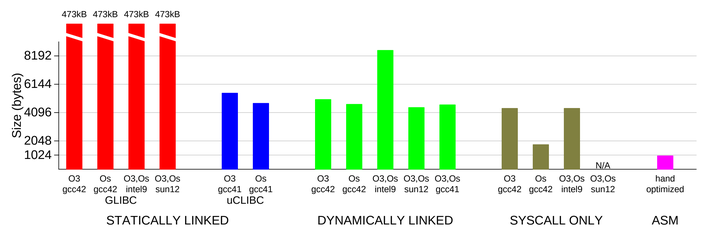


Architectural Size Correlations

0.9020	Minimum possible instruction size
0.8652	Number of integer registers
0.6623	Architecture has a zero register
0.5845	Bit-width
-0.4366	Hardware divide in ALU
0.4385	Number of operands in each instruction
-0.3356	Unaligned load/store available
0.2773	Year the architecture was introduced
-0.2597	Auto-incrementing addressing scheme
-0.2597	Hardware status flags (zero/overflow/etc.)
-0.1252	Little or Big endian
-0.0487	Branch delay slot
-0.0079	Maximum possible instruction size

Other Considerations

System libraries and compiler overhead can overshadow the effects of size optimization, increasing memory footprint by several orders of magnitude. These effects cannot be ignored when analyzing system-wide code-density.



Future Work

- Investigate more architectures.
- Evaluate performance impact of dense architectures.
- Propose compact architectures for FPGA and GPU-based systems.