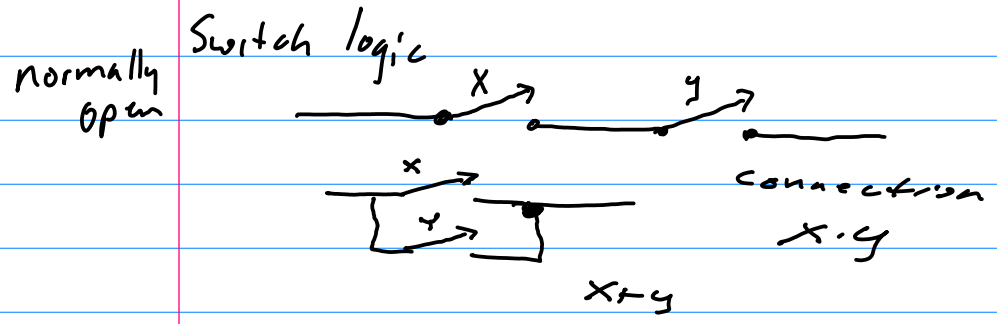
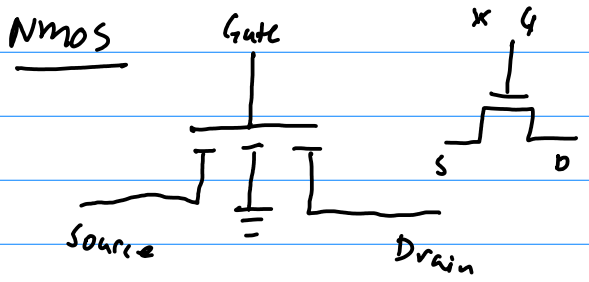
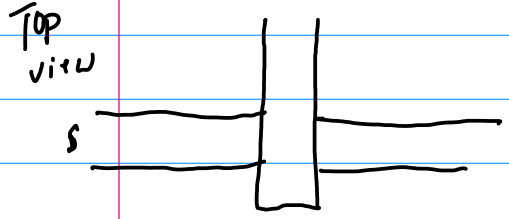
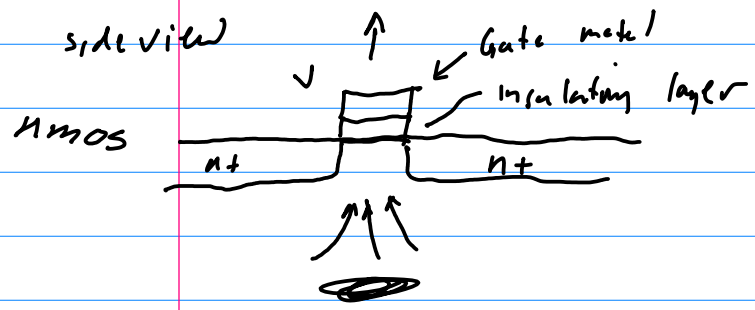
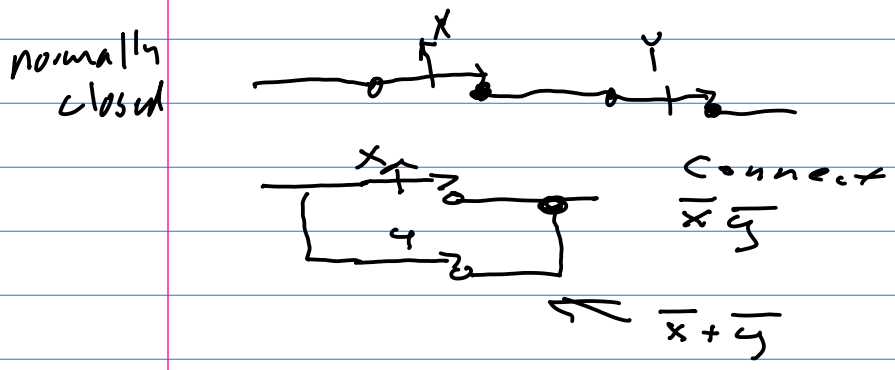
Implementation Technology

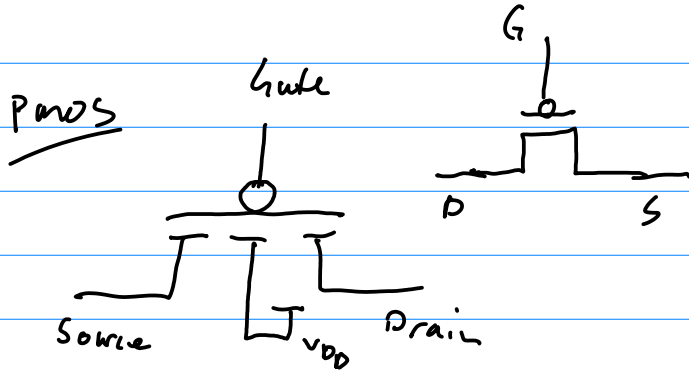


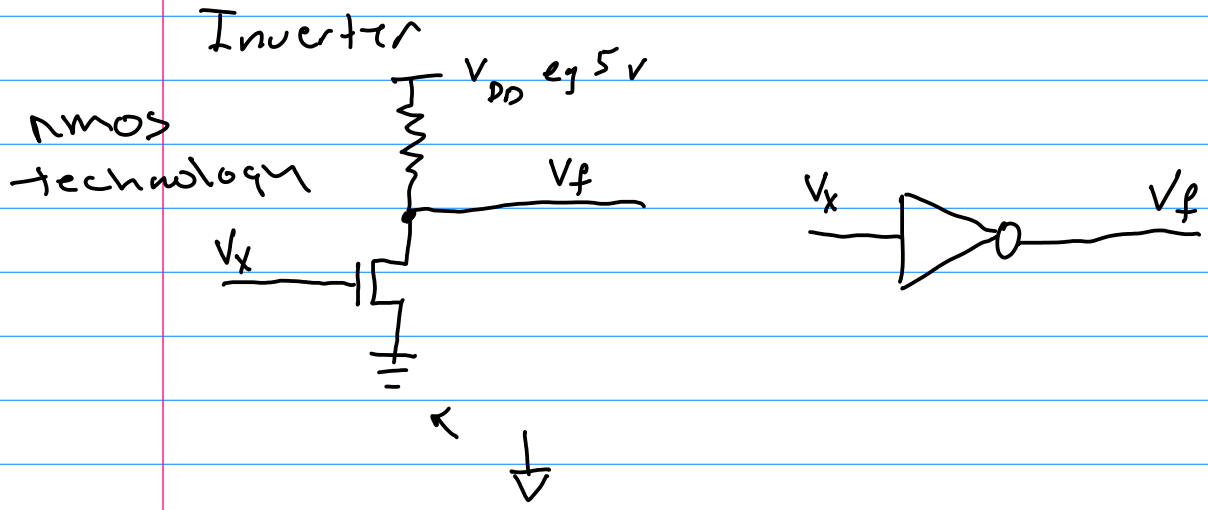




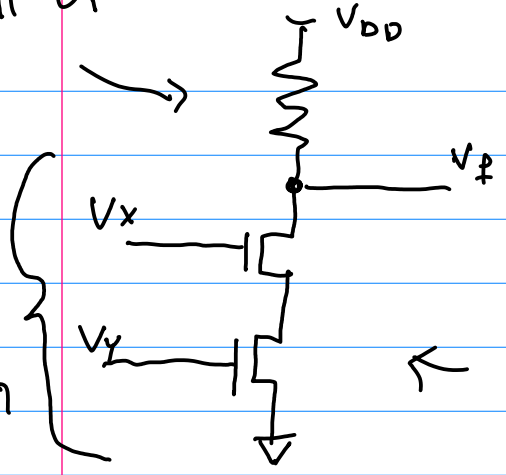








Pull UP



Pull Down network

V_x	V_y	V_f
L	L	H
L	H	H
H	L	H
H	H	L

Positive Logic

X	Y	f
0	0	1
0	1	1
1	0	1
1	1	0

NAND

Negative logic

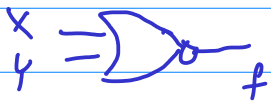
X	Y	f
1	1	0
1	0	0
0	1	0
0	0	1

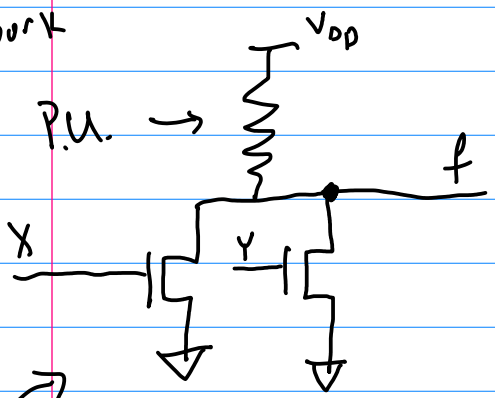
NOR

$\bar{x}\bar{y}$

$\overline{x+y}$

NAND



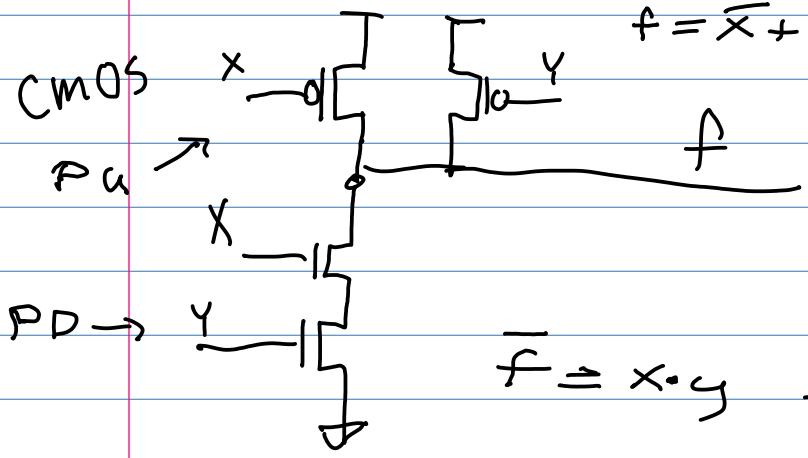


Pull Down Network

X	Y	f
0	0	1
0	1	0
1	0	0
1	1	0

NOR

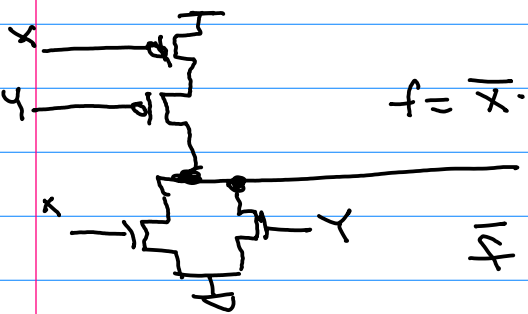
Resistor



$f = \bar{x} + \bar{y}$ -> function is true

NAND

$\bar{f} = x \cdot y$ function is zero



$f = \bar{x} \cdot \bar{y}$ NOR

$\bar{f} = x + y$

use only

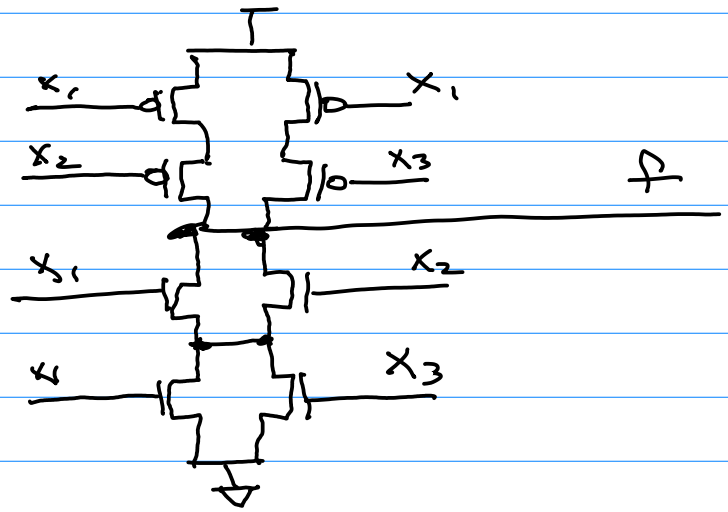
PMOS works poorly in P.D. → in PU

NMOS works poorly in P.U. in PD

① Complex CMOS

$\rightarrow f = \overline{x_1}\,\overline{x_2} + \overline{x_1}\,\overline{x_3}$

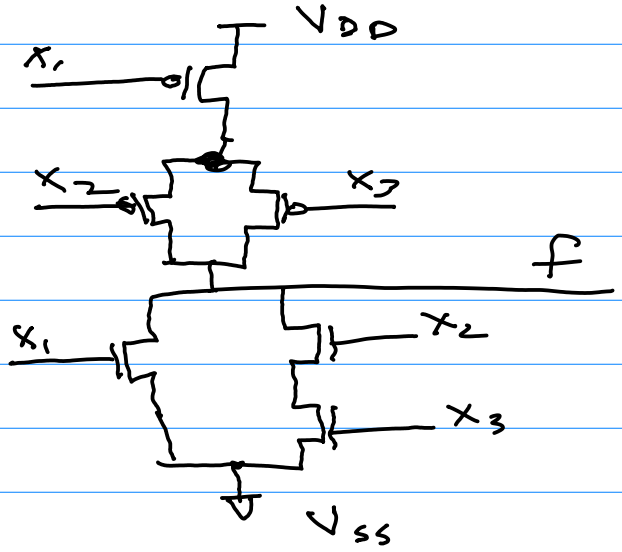
$\overline{f} = (x_1 + x_2)(x_1 + x_3)$



② Better

$f = \overline{x_1}\,(\overline{x_2} + \overline{x_3})$

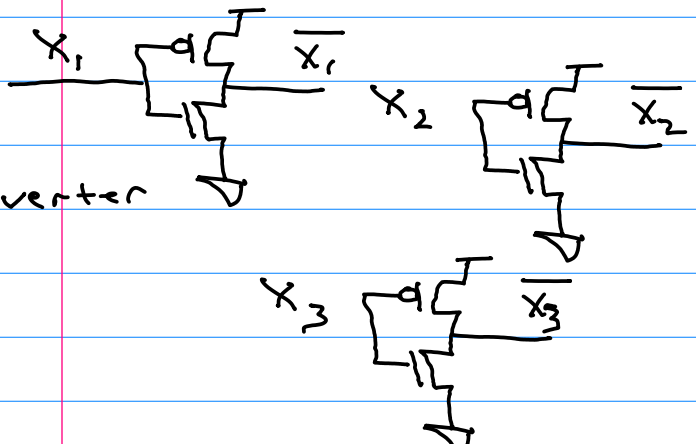
$\overline{f} = x_1 + x_2 x_3$

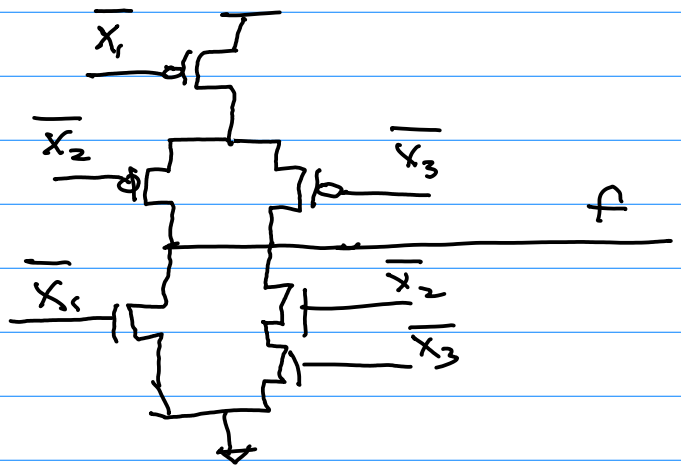


③

$f = x_1 (x_2 + x_3)$

$\overline{f} = \overline{x_1} + \overline{x_2}\,\overline{x_3}$

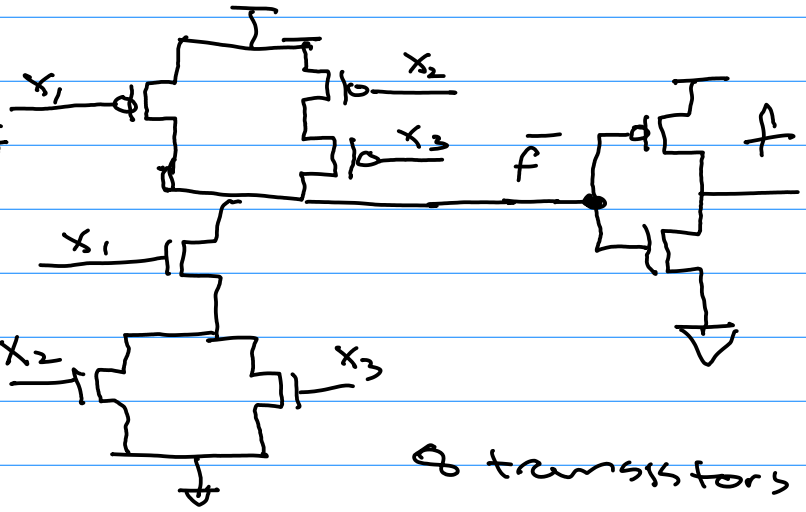




12 transistors

$f = x_1(x_2 + x_3)$ ← PD $\bar{f}$

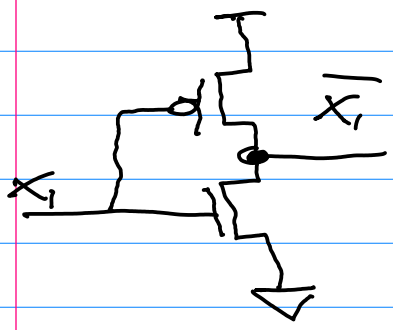
$\bar{f} = \bar{x}_1 + \bar{x}_2\bar{x}_3$ ← PU $\bar{f}$

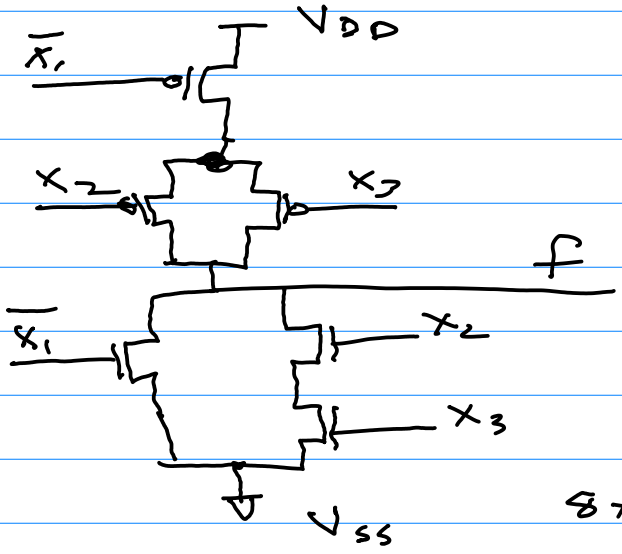


8 transistors

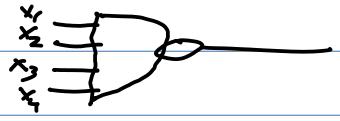
$f = x_1(\bar{x}_2 + \bar{x}_3)$

$\bar{f} = \bar{x}_1 + x_2x_3$





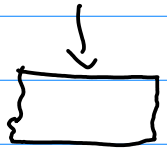
8 transistors



$f = \overline{x_1 x_2 x_3 x_4}$

$= \bar{x}_1 + \bar{x}_2 + \bar{x}_3 + \bar{x}_4$

$\bar{f} = x_1x_2x_3x_4$



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