1) 11110100 → Decimal

Assume a) 2's complement

11110100 → 1's complement → 00001011 → +1 → 00001100 ← +12 ← −12

b) Sign-magnitude

Sign | magnitude

11110100 → 1110100

64 32 16 8 4 2 1

↓

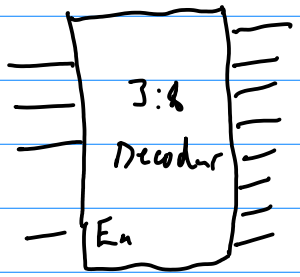
−116

7×16 + 4

112 + 4 = 116

2) What device generates "one-hot" encoding from 3 inputs? Draw

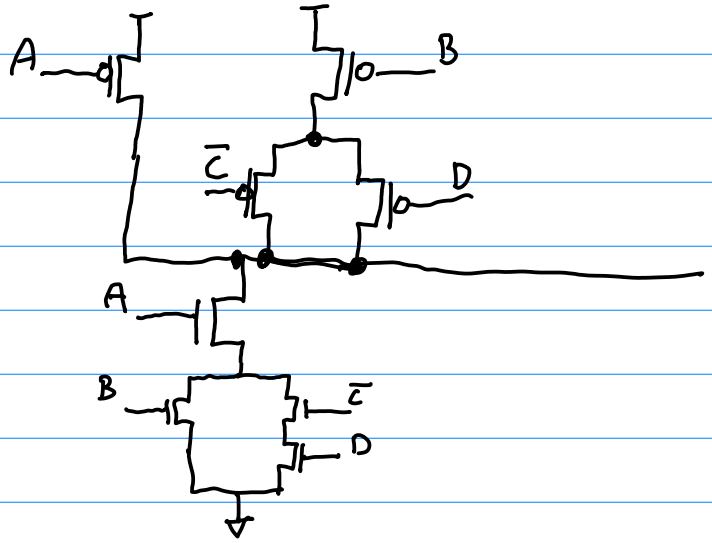
Decoder

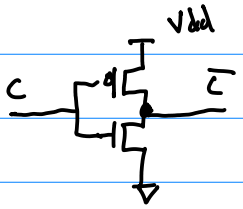


3) Draw Complex CMOS to implement $\bar{A} + \bar{B}(C + \bar{D})$ with minimal transistors you may put inverters on inputs or output but draw them & put them in the count

1 → $f = \bar{A} + \bar{B}(C + \bar{D})$ PU ← PMOS

0 → $\bar{f} = A \cdot (B + \bar{C}D)$ PD





10 transistors

4) Fan in / Fan out & noise margin

74H00 driving a 74LS00 (two-input NANDs)

Noise margin

$NM_L = V_{IL_{LS}} - V_{OL_H} = .8 - .4 = .4$ ✓

$NM_H = V_{OH} - V_{IH} = 2.4 - 2 = .4$ ✓

Fan Out $FO_L = \left| \frac{I_{OL(H)}}{I_{IL(LS)}} \right| = \frac{20}{.4} = 50$

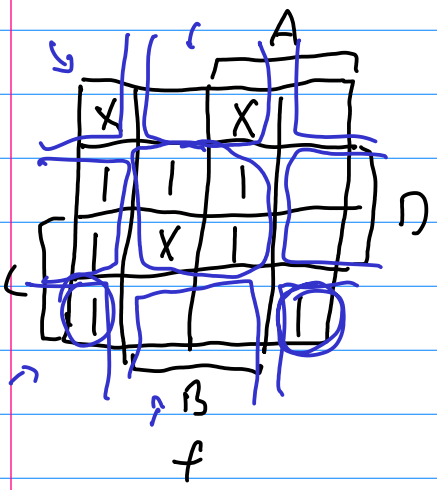
$FO_H = \left| \frac{I_{OH(H)}}{I_{IH(LS)}} \right| = \frac{500}{20} = 25$

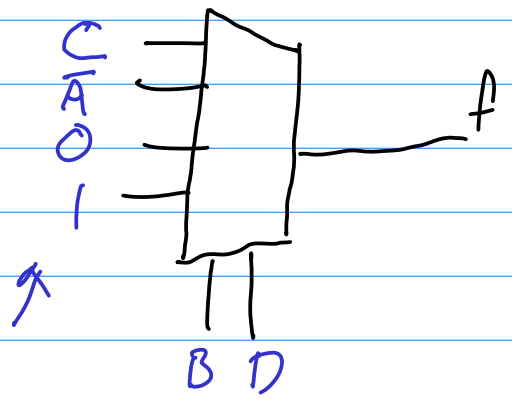
$FO = \min(FO_L, FO_H) = \min(50, 25) = 25$

5) What is the fan-in for the 74LS00 NAND?

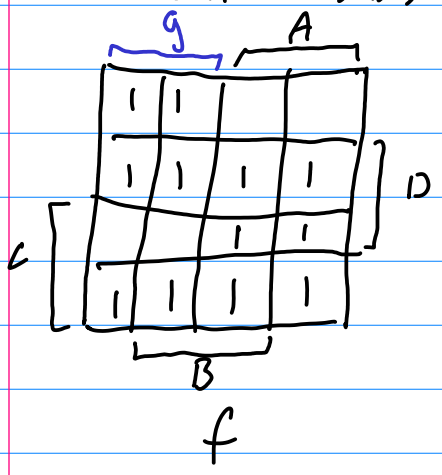
2

6) Implement using a 4:1 mux & no other logic





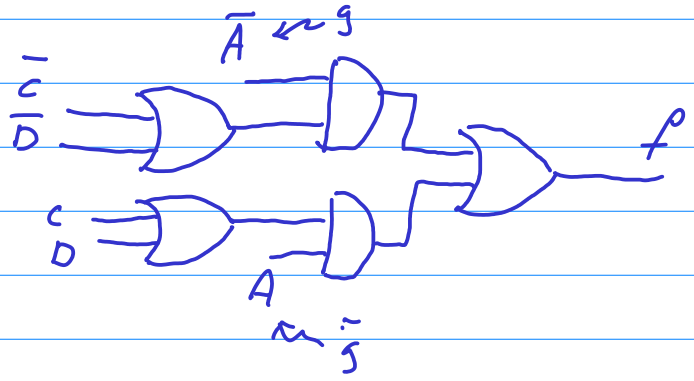
7) Functional Decomposition to derive a multi-level circuit max fan-in of two



first two columns are the same - call them g

$g = \bar{A}$ ← when g is true

Now $f = g \cdot (\bar{C} + \bar{D}) + \bar{g} \cdot (C + D)$ ← when g is false



8) What is the difference between an asynchronous and synchronous clear on a flip-flop

asynchronous - clears now

synchronous - clears on clock signal

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54 SERIES 74 '00, '04, '10, '20, '30			SERIES 54H SERIES 74H 'H00, 'H04, 'H10, 'H20, 'H30			SERIES 54L SERIES 74L 'L00, 'L04, 'L10, 'L20, 'L30			SERIES 54LS SERIES 74LS 'LS00, 'LS04, 'LS10, 'LS20, 'LS30			SERIES 54S SERIES 74S 'S00, 'S04, 'S10, 'S20, 'S30, 'S133			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	54 Family			−400			−500			−100			−400			−1000	μA
	74 Family			−400			−500			−200			−400			−1000	
Low-level output current, I_{OL}	54 Family			16			20			2			4			20	mA
	74 Family			16			20			3.6			8			20	
Operating free-air temperature, T_A	54 Family	−55		125	−55		125	−55		125	−55		125	−55		125	°C
	74 Family	0		70	0		70	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SERIES 54 SERIES 74 '00, '04, '10, '20, '30			SERIES 54H SERIES 74H 'H00, 'H04, 'H10, 'H20, 'H30			SERIES 54L SERIES 74L 'L00, 'L04, 'L10, 'L20, 'L30			SERIES 54LS SERIES 74LS 'LS00, 'LS04, 'LS10, 'LS20, 'LS30			SERIES 54S SERIES 74S 'S00, 'S04, 'S10, 'S20, 'S30, 'S133			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	1, 2			2			2			2			2			2			V
V_{IL}	Low-level input voltage	1, 2		54 Family			0.8			0.8			0.7			0.7			0.8	V
				74 Family			0.8			0.8			0.7			0.8			0.8	
V_{IK}	Input clamp voltage	3	V_{CC} = MIN, I_I = §				−1.5			−1.5						−1.5			−1.2	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IL} = V_{IL} max, I_{OH} = MAX	54 Family	2.4	3.4		2.4	3.5		2.4	3.3		2.5	3.4		2.5	3.4		V
				74 Family	2.4	3.4		2.4	3.5		2.4	3.2		2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V	I_{OL} = MAX, 54 Family		0.2	0.4		0.2	0.4		0.15	0.3		0.25	0.4			0.5	V
				I_{OL} = MAX, 74 Family		0.2	0.4		0.2	0.4		0.2	0.4		0.25	0.5			0.5	
				I_{OL} = 4 mA, Series 74LS												0.4				
I_I	Input current at maximum input voltage	4	V_{CC} = MAX	V_I = 5.5 V			1			1			0.1						1	mA
				V_I = 7 V												0.1				
I_{IH}	High-level input current	4	V_{CC} = MAX	V_{IH} = 2.4 V			40			50			10							μA
				V_{IH} = 2.7 V												20			50	
I_{IL}	Low-level input current	5	V_{CC} = MAX	V_{IL} = 0.3 V									−0.18							mA
				V_{IL} = 0.4 V			−1.6			−2						−0.4				
				V_{IL} = 0.5 V															−2	
I_{OS}	Short-circuit output current◆	6	V_{CC} = MAX	54 Family	−20		−55	−40		−100	−3		−15	−20		−100	−40		−100	mA
				74 Family	−18		−55	−40		−100	−3		−15	−20		−100	−40		−100	
I_{CC}	Supply current	7	V_{CC} = MAX		See table on next page															mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§I_I = −12 mA for SN54'/SN74', −8 mA for SN54H'/SN74H', and −18 mA for SN54LS'/SN74LS' and SN54S'/SN74S'.
◆Not more than one output should be shorted at a time, and for SN54H'/SN74H', SN54LS'/SN74LS', and SN54S'/SN74S', duration of short-circuit should not exceed 1 second.