ECE-342 Lab 5: BJT Amplifier
Sample Lab Report

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Abstract

The design and test of a common-emitter BJT amplifier is described. The amplifier uses two NPN transistors to form a current-source bias network, and a single 2N2222A NPN transistor as the common-emitter amplifier. The amplifier requires $+10 \, \text{V}$ and $-5 \, \text{V}$ supplies, and achieved a measured 46.5 dB gain with 7.8 kΩ input impedance at 1 kHz, and 1.2 MHz 3-dB Bandwidth. Component selection and test procedures are described.
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1 Introduction

This report describes the design, implementation and test of a common-emitter amplifier using 2N2222A NPN BJT transistors. A two-transistor current source is used to provide the required bias current for the single-transistor common-emitter amplifier. The amplifier requires +10 V and −5 V supplies, and is designed to achieve a nominal “mid-band” gain of 46 dB. Specific Lab 5 requirements are summarized in the Lab 5 Assignment sheet, included as Appendix A. The amplifier was constructed using a solderless breadboard, and lab measurements verify that the amplifier achieved a peak gain of 46.5 dB at 5 kHz, with 3-dB band ranging from 73 Hz to 1.2 MHz.

Section 2 describes the development of the amplifier, including the selection of components and the prediction of the lower cutoff frequency. Circuit simulation results are presented in Section 3, and experimental measurements and procedures are presented in Section 4. Section 5 gives a summary and comparison of the simulated and measured results, and addresses specific questions associated with the lab assignment.

2 Circuit Development and Analysis

A schematic of the amplifier is shown in Figure 1. In the schematic, resistor $R_1$ and transistors $Q_1$ and $Q_2$ form a current source used to determine the bias current $I_{C3}$. $Q_3$ and $R_L$ form the common-emitter amplifier, and the capacitor $C$ is used to essentially ground the emitter of $Q_3$ as the signal frequency increases.

The circuit design proceeds as follows: First, the required bias current $I_{C3}$ and resistor value $R_L$ are determined by assuming that the capacitor acts as a short at signal frequencies. Second, the current source components are determined to provide the required bias current $I_{C3}$. Finally, the effect of the capacitor $C$ is examined by including its finite impedance in the small-signal analysis. These design steps are presented in Sections 2.1, 2.2, and 2.3 respectively.

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Figure 1: Circuit schematic for the common-emitter BJT amplifier.

**Design Requirements:**
- Amplifier Gain: 46 dB
- $1 \text{k}\Omega \leq R_L \leq 10 \text{k}\Omega$
- $47.1 \mu\text{F} \leq C \leq 100 \mu\text{F}$

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Required Section: Give an overview of the lab, and a short outline of the report that will follow. Generally avoid equations. (Leave the details to later sections.) Do give a preview of the results. Your report should stand on its own. Do not assume that the reader has assignment sheet.

Most of your labs will include some design choices, so a section similar to this should be included in the report.

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1The Lab 5 assignment actually specified 2N3904 NPN transistors. The 2N2222A device was substituted for this lab because the 2N3904 devices were out of stock.
2.1 CE Amplifier: Selection of $R_L$ and $I_{C3}$

Figure 2 shows the common-emitter amplifier with an ideal current source replacing the bias network of the original schematic. The corresponding small-signal model of the circuit is also shown. The model is based on the assumptions that the capacitor impedance is small at the input signal frequencies (and may be considered a short), and the transistor output resistance $r_o$ is large compared to $R_L$, and may be neglected. The small signal parameters are

$$g_m = \frac{I_{C3}}{V_T}$$

$$r_\pi = \frac{\beta}{g_m},$$

where $V_T \approx 25.8$ mV is the thermal voltage, and $\beta$ is the current gain of $Q_3$. Circuit analysis of the small signal model yields the amplifier gain

$$A_{vo} = \frac{v_{out}}{v_{in}} = -g_m R_L.$$  \hspace{1cm} (3)

To achieve the desired gain of 46 dB, set $g_m R_L = 200$. Substituting (1) into this gives the required relationship between $R_L$ and the bias current $I_{C3}$:

$$I_{C3} = \frac{200 V_T}{R_L} \approx \frac{5.16}{R_L}$$ \hspace{1cm} (4)

There are many valid choices for $R_L$ and $I_{C3}$. This report describes the minimum power choice, in which the value of $R_L$ is made to be as large as possible.

$$R_L = 10 \, \text{k}\Omega \quad I_{C3} = 0.516 \, \text{mA}$$ \hspace{1cm} (5)

Regardless of the selection of $R_L$, setting $I_{C3} = 5.16/R_L$ implies that the DC drop across $R_L$ will be 5.16 V. So the DC component of $v_{OUT}$ will be $V_{out} = 10 - 5.16 = 4.84$ V. The selection of $R_L$ does not change the output dynamic range.

The input resistance of the amplifier is

$$R_{in} = r_\pi = \frac{\beta}{g_m} = \frac{\beta(R_L/200)}{g_m}.$$ \hspace{1cm} (6)

Selecting a large value of $R_L$ has increased the input resistance. The actual value is difficult to predict, since the 2N2222A transistor only specifies $\beta > 50$ (at $I_c = 1$ mA). Using $R_L = 10$ k$\Omega$ gives

$$R_{in} \geq 2.5 \, \text{k}\Omega $$ \hspace{1cm} (7)

2.2 Design of the Current Source: Selection of $R_1$

Referring back to Figure 1, the value of $R_1$ is determined to provide the desired value of $I_{C3} = 0.516$ mA. Since the actual value of $\beta$ cannot be anticipated, the design here is based on a large-\$\beta\$ approximation. All base currents are assumed to be negligible. In this case, the design goal is

$$I_{C2} = I_{C3} = 0.516 \, \text{mA}.$$ \hspace{1cm} (8)
Figure 2: The common-emitter amplifier with bias network replaced by an ideal current source, and the corresponding small-signal model.

Figure 3: The small-signal model of the amplifier including the capacitor impedance.

The base-emitter voltages of $Q_1$ and $Q_2$ are tied together. If the transistors are matched to each other, the currents $I_{C2}$ and $I_R$ must also agree. The resistor $R_1$ determines $I_R$, and the transistor $Q_2$ reproduces this current as $I_{C2} = I_R$.

If $Q_1$ and $Q_2$ are both forward active,

$$v_{BEQ_1} = v_{BEQ_2} \approx 0.7 \text{ V}.$$  \hspace{1cm} (9)

The voltage drop across $R_1$ is approximately 4.3 V, so $R_1$ is determined by

$$I_R = 0.516 \text{ mA} = \frac{4.3 \text{ V}}{R_1} \hspace{1cm} (10)$$

$$R_1 = 8.33 \text{ k}\Omega.$$ \hspace{1cm} (11)

2.3 Low-Frequency Performance: Selection of $C$

The low-frequency behavior of the amplifier is predicted by including the impedance of the capacitor in the small-signal analysis. The resulting small-signal model is shown in Figure 3.

The transfer function of the amplifier is determined by observing that the input current is given by $v_{be}/r_\pi$. $v_{in}$ and $v_{be}$ are related by adding the voltages across $r_\pi$ and across the
capacitor.
\[ v_{in} = v_{be} + \frac{1}{C_s} \left( v_{be}/r_\pi + g_m v_{be} \right) \] (12)

Solving for \( v_{be} \) gives
\[ v_{be} = v_{in} \left( \frac{1}{1 + g_m/C_s + 1/(r_\pi C_s)} \right) \approx v_{in} \left( \frac{1}{1 + g_m/C_s} \right). \] (13)

The approximation is justified by \( r_\pi = \beta/g_m \), so the third term of the denominator is a factor of \( \beta \) smaller than the second term. The output voltage is then
\[ v_{out} = -g_m R_L v_{be} = v_{in} \left( \frac{-g_m R_L}{1 + g_m/C_s} \right). \] (14)

The system transfer function is a high pass characteristic
\[ \frac{v_{out}}{v_{in}} = (-g_m R_L) \left( \frac{s}{s + g_m/C_s} \right). \] (15)

The capacitor \( C \) determines the lower 3-dB cutoff frequency \( \omega_3 = g_m/C \). For this lab, the lower band edge was not specified, and a value of \( C = 47.1 \mu F \) was selected based upon available components. Using \( I_{C3} \) from (5) gives
\[ g_m = \frac{0.516 \text{ mA}}{25.8 \text{ mV}} = 0.02 \ \Omega^{-1} \] (16)
\[ \omega_3 = \frac{0.02 \ \Omega^{-1}}{47.1 \ \mu F} = 424 \ \text{rad/s} \] (17)
\[ f_3 = \frac{\omega_3}{2\pi} = 67.6 \ \text{Hz}. \] (18)

3 Simulated Performance

Circuit simulations were performed using the Micro-Cap circuit simulator. Simulations using the component values derived in Section 2 \( (R_L = 10 \ \text{k}\Omega, R_1 = 8.33 \ \text{k}\Omega, C = 47.1 \ \mu F) \) showed an amplifier gain of 45.7 dB, 0.3 dB lower than the desired gain of 46 dB. This 3% error in \( v_{out}/v_{in} \), is in part a result of neglecting the transistor output impedance \( r_o \) in Section 2. For the collector current of 0.516 mA, the \( r_o \) of transistor \( Q_3 \) is approximately 200 k\( \Omega \) (based upon \( V_A = 100 \text{ V} \) taken from the SPICE model for the 2N2222). Including this value in the small-signal analysis gives a 5% reduction in the calculated gain. Also, the approximate 0.7 V base emitter voltage of \( Q_1 \) was slightly high relative to the simulation, causing the gain to be underestimted by approximately 2%.

The gain of the circuit can be increased by increasing \( R_L \) (not allowed in this lab beyond 10 k\( \Omega \)), or by decreasing \( R_1 \). By decreasing \( R_1 \), the bias currents are increased, and the transconductance \( g_m \) of \( Q_3 \) increases. Trial and error indicated that using \( R_1 = 8.0 \ \text{k}\Omega \) results in a gain of 46 dB.

Based on the simulation results, hardware components were selected with values close to the desired values of \( R_1 = 8 \ \text{k}\Omega, R_L = 10 \ \text{k}\Omega, \text{ and } C = 47.1 \ \mu F \). The actual component values for the implementation are listed in Table 1. The corresponding simulated gain and 3-dB corner frequencies are also indicated in the table. More detailed plots of the simulated performance are given in Section 4, where the simulated curves (using these measured component values) are presented with the hardware measurements.
Table 1: Measured component values used in the hardware implementation, and the corresponding (simulated) amplifier gain, 3-dB corner frequencies, and input impedance.

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_1$</td>
<td>7.915 kΩ</td>
</tr>
<tr>
<td>$R_L$</td>
<td>9.996 kΩ</td>
</tr>
<tr>
<td>$C$</td>
<td>47.1 µF</td>
</tr>
</tbody>
</table>

- Peak gain (at 8.28 kHz) = 46.06 dB
- Lower 3-dB corner frequency = 70.1 Hz
- Upper 3-dB corner frequency = 719.7 kHz
- Input Impedance $|v_{in}/i_{in}| = 4.6$ kΩ at 1 kHz

Figure 4: Final schematic diagram of the amplifier showing measured component values.

4 Experimental Implementation

Figure 4 shows the final schematic of the amplifier indicating the measured values of all components.

The capacitor “C” was actually implemented as two capacitors in parallel: a 47 µF electrolytic capacitor, and a 0.1 µF ceramic capacitor. The ceramic capacitor was included to improve the performance of the system at high frequencies, where the electrolytic capacitor fails. Additional circuitry used to create the input signal $v_{in}$ and to measure the output signal $v_{out}$ are discussed in Sections 4.1 and 4.2 respectively.

4.1 Generation of the input signal

An Agilent 33120A function generator was used to provide the amplifier input signal for test. The generator has a 50 Ω output impedance, and can produce a sinusoidal output at amplitudes down to 50 mV peak-to-peak to a matched load (50 mV peak to a high impedance load). To test this amplifier with 46 dB of gain, much smaller input signals are required. A resistor voltage divider was used to produce a low-level signal at a much lower output impedance. Resistors with nominal values of 150 Ω and 1 Ω were used to give an output amplitude which was $\approx 1/200^{th}$ of the function generator setting with an output impedance of approximately 1 Ω. Figure 5 gives the schematic showing the actual
Thevenin Equivalent

Function Generator

Input Signal Source

To Amplifier

(resistor values used. For all tests, the function generator amplitude was set to provide a 5 mV peak-to-peak sinusoidal input \(v_{in}\) to the amplifier.

Simulations predict that the amplifier input impedance will remain above 80 Ω over the entire range of test frequencies. Since the source impedance for this input configuration is low (\(\approx 1 \Omega\)), the amplifier input amplitude should remain at a nearly constant level as the input frequency is adjusted. For test, the amplifier input level was verified at 1 kHz using an oscilloscope, and the scope was disconnected from the input at high frequencies. This ensures that the amplifier would not be effected by the capacitive loading of the scope probe.

4.2 Measurement of the output signal

An HP 54603B oscilloscope was used to measure output signal levels. However, the scope input presents a capacitive load to the circuit of approximately 13 pF. Including this load in the simulation significantly changed the bandwidth of the amplifier. (Without the scope probes, the simulated upper 3-dB frequency of the amplifier was 720 kHz. With the probe connected directly to the output, the upper 3-dB bandwidth dropped to 468 kHz.)

To avoid problems associated with loading the amplifier with the scope probe, an emitter-follower was used to buffer the output signal to the oscilloscope. Figure 4 shows the schematic of the output signal buffer. Simulations were used to verify that probing the buffer output \(v_{out2}\) did not significantly change the amplifier performance, and that signal gains calculated based on \(v_{out2}\) were virtually indistinguishable from those calculated from \(v_{out}\).

4.3 Measurement results

Figure 6 shows a plot of the amplifier gain for frequencies ranging from 10 Hz to 10 MHz. Hardware measurements are indicated by the plot symbols, while the plotted curve shows the results of the Micro-Cap simulation. Measured results are all for a 5 mV peak-to-peak
input signal ($v_{in}$). At each frequency, the peak-to-peak amplitude of $v_{out2}$ was measured using the oscilloscope, and used to calculate the gain.

Figure 7 shows a plot of the amplifier input impedance over the same band of frequencies. Again, the measurements are indicated by plot symbols, while the plotted curve represents the results of the simulation. To measure the input impedance of the amplifier, a 10 kΩ resistor was inserted between the signal source and the amplifier input. The peak-to-peak amplitude of $v_{out2}$ was then measured ($V_{10k}$), and compared to the value obtained without the 10 kΩ resistor ($V_0$). The attenuation indicates the signal loss at the amplifier input. If $R_{in}$ is the amplifier input, then

$$\frac{V_{10k}}{V_0} = \frac{R_{in}}{R_{in} + 10 \text{ kΩ}}.$$  \hfill (19)

$$R_{in} = \left( \frac{V_{10k}/V_0}{1 - V_{10k}/V_0} \right) \times (10 \text{ kΩ}).$$  \hfill (20)

5 Discussion

In general, the experimental results agree reasonably well with the simulation predictions. Table 2 summarizes specific amplifier specifications.

The gain of the hardware implementation was 0.5 dB higher than the predicted value of 46 dB. This 0.5 dB deviation corresponds to a 6% error in the value of $v_{out}/v_{in}$. The error could be caused by mis-matches between transistors $Q_1$ and $Q_2$ (changing the bias current), or by an imperfect SPICE model for transistor $Q_3$. The error is larger than would be expected from measurement error for the test equipment used.
Figure 7: Amplifier input impedance. The solid curve shows the results of the Micro-Cap simulation, while the plot symbols indicate measured data.

Table 2: Amplifier performance summary, including design goals, simulated performance, and measured performance.

<table>
<thead>
<tr>
<th></th>
<th>Design</th>
<th>Simulation</th>
<th>Measured</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak Gain</td>
<td>46.0 dB</td>
<td>46.06 dB</td>
<td>46.5 dB</td>
</tr>
<tr>
<td>Lower 3-dB Corner</td>
<td>70.1 Hz</td>
<td>73 Hz</td>
<td></td>
</tr>
<tr>
<td>Upper 3-dB Corner</td>
<td>719.7 kHz</td>
<td>1.2 MHz</td>
<td></td>
</tr>
<tr>
<td>Input Resistance (@ 1 kHz)</td>
<td>4.6 kΩ</td>
<td>7.82 kΩ</td>
<td></td>
</tr>
</tbody>
</table>
While the lower 3-dB frequency of the implementation agreed closely with the simulation result, the upper cutoff frequency of 1.2 MHz was significantly larger than the value predicted by the simulation. The upper cutoff frequency is determined by the parasitic capacitance of transistor $Q_3$. Apparently the values incorporated in SPICE model were larger than those of the device that was used in the implementation.

Since the amplifier input impedance $R_{in}$ depends upon the $\beta$ of $Q_3$, it is not surprising that the simulated and measured results differ from each other. Both results (at 1 kHz) satisfy the prediction of (7), and are reasonable for the transistors used. Some care should be taken in interpreting Figure 7 at other frequencies. Simulation results show that the impedance is resistive only for frequencies in the range $300 \text{ Hz} \leq f \leq 3 \text{ kHz}$. At frequencies below or above this band, the amplifier input impedance is primarily capacitive. At high frequencies in particular, the impedance magnitude is much smaller than that predicted by (7).

6 Conclusion

The design and implementation of a 46 dB, 1.2 MHz bandwidth amplifier has been presented. Hardware tests verified the performance of the amplifier. While the amplifier performed largely as predicted, some care is needed in interfacing to the amplifier. The amplifier bandwidth is seen to be sensitive to small capacitive loads at the output (e.g. 13 pF scope probe). Also, the amplifier input impedance varies with frequency over several orders of magnitude. The measured 1.2 MHz bandwidth was achieved only after buffering the output signal and creating a low-impedance input source.
A Lab 5 Assignment

ECE-342 Fall 2006, Lab 5: BJT amplifier
Due Wed. 12/6, 5:00 PM

1 Overview
The amplifier shown below utilizes a current source from lab 4 to appropriately bias the transistor Q3. In designing the circuit, assume that the signal vs does not contain any DC offset.

The capacitor C will ultimately determine the low-frequency behavior of the amplifier. It is selected so that at “typical” signal frequencies, the impedance of the capacitor is small, and the emitter of Q3 is essentially grounded.

The amplifier voltage gain is assumed to be measured at these “mid-band” frequencies (frequencies above those where the impedance of the capacitor is significant, but below those where the parasitic capacitors of the BJTs become significant).

2 Tasks
Use 2N3904 transistors for Q1, Q2, and Q3.

1. Complete the design of the amplifier to give a voltage gain of 46 dB. Provide the maximum possible output dynamic range. You should specify all component values, but your selections must meet the constraints:

   \[ 1 \, \text{k}\Omega \leq R_L \leq 10 \, \text{k}\Omega \]
   \[ 10 \, \mu\text{F} \leq C \leq 100 \, \mu\text{F} \]

   Simulate your design, noting the actual (mid-band) gain and dynamic range. Construct and verify the performance of the amplifier.

2. Determine the input resistance of your final design. Discuss how your choice of biasing influences the input resistance.

3. Use a small-signal equivalent circuit to predict the lower cutoff frequency of the amplifier. Verify by simulation and experimentally.

Use appendices for anything that does not fit into the normal writeup format. If there are specific questions in the lab assignment that are not easily addressed in the normal write-up, then this is a good place to address them.

For this sample report, the assignment sheet is attached here to provide some frame of reference. IT IS NOT REQUIRED for your lab reports. (We have lots of copies of the lab assignment.)
Every ECE342 Lab will include a form similar to the one shown here, with signatures indicating that tasks were completed on time, and lab notebooks have been reviewed. Turn in this (completed) form with your report.
C General Notes for ECE-342/3 Lab Reports

Checklist

• Typesetting Requirements:
  – Use a 12 point font.
  – Single space the text.
  – Use a 6 inch line length: 0.5 inch left margin, and 2 inch right margin (for grader comments).
  – Number the pages, and include table of contents.
  – Figure captions should be placed below the figure. Table captions should be placed above the tables.
  – All Figures/Tables should be discussed within the text of the report. Try to place the Figures/Tables near the discussion.

• Complete all of the tasks associated with the lab. Is it easy for the grader to find each task?

• Be concise and clear. Don’t over-explain the theory behind the devices or equations. Stay on task with the lab assignment.

• Summarize your results! Make sure the reader understands the main points of what you’ve presented.

• Be technically accurate. If you have questions, ask.

• Clearly distinguish between simulated and experimental results.

• Use good grammar.

• Use good lab technique. Consider the effect of the instrumentation (scope capabilities, function generator output impedance, etc.) on your measurements.

• If your results are not as expected, then follow up if possible. For example, if you expect that the scope probe changes the performance, then (at least!) include the probe in a simulation and see if it reproduces your observations.

• Include units on any numerical values. Use symbols instead of spelling out words. (Use “10 kΩ” instead of “10 kohm”.)

• Use subscripts where appropriate. (Use “R₂” instead of “R2”).

• Avoid large tables of numerical data. Present a chart or graph of the data instead. If you need to have a record of the numerical data for some reason, put it in an appendix.

• There’s no need to include data-sheets or other reference information in the report.

• Make your graphs clear. Axes should be labeled, and units should be indicated.

• Make sure that your notation is consistent. Don’t change notation from section to section, or between the text and graphs/tables. Be especially careful about graphs/tables for which axis labels are automatically generated.
**First Person/Third Person**

There will always be exceptions, but unless it’s your diary (or a lab notebook), there will rarely be a reason to use the first-person presentation in a lab report. In general, stick to the third-person presentation (unless there really is some reason that you personally should be the subject of an idea). Instead of “We considered five options:...”, use “Five options are considered:...”. Think about what the subject of the sentence *should* be. (In this case, is the subject “We”, or should it be the “options”?)

**Active/Passive Voice**

In the active voice, the subject of the sentence is performing the action of the verb. In contrast, for the passive voice the subject receives the action of the verb. Both are common in technical writing.

In general, active sentences are shorter and more powerful than passive sentences. They use stronger verbs, and tend to make written material more engaging (less boring). Given a choice, use the active voice.

Writers often choose the passive voice deliberately when they want to focus on the object, or obscure the person performing the action. In technical documents, the passive voice is often selected as a means of avoiding a first-person presentation.

Consider these three variations:

1. “The data were analyzed to show that...” (Not bad, Third person, but passive)
2. “We analyzed the data to show that...” (Avoid. Active, but first person.)
3. “Data analysis shows that...” (Best. Active, third person.)

Only option 3 really gets the subject (“Data analysis”) correct. It seems that the subject in option 2 (“We”) is not central to the ideas being presented, and does not really belong.