SOLID-STATE NANOPORE CHARACTERIZATION AND LOW NOISE TRANSIMPEDEANCE AMPLIFIER FOR NANOPORE-BASED GENE SEQUENCER

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The detection and identification of a particle transported in an aqueous solution through a nanopore (≤10nm opening in a thin dielectric membrane) is of technological importance and has various applications. For example, in a DNA nano-sequencer, an electrical signal is generated when a single strand of DNA passes through the nanopore. This signal is amplified by a transimpedance amplifier, then converted to a digital signal representing one of the four possible bases in the DNA. There are many challenges in implementing this sequencer. One of the challenges is to design a transimpedance amplifier with sufficient bandwidth and sensitivity to correctly identify each nucleotide.

In this work the I-V characteristics of a solid-state nanopore are determined. A low–noise transimpedance amplifier was designed to increase the magnitude of the electrical signals for further signal analysis. The transimpedance amplifier, designed in 240nm IBM BiCMOS process, has an input capacitance of 250fF, a gain of 120dB, a bandwidth of 4MHz and a minimum input referred noise of 130fA/√Hz. Power dissipation is 17.7mW.
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<th>Description</th>
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<tr>
<td>$A_n$</td>
<td>Noise gain</td>
</tr>
<tr>
<td>$A_o$</td>
<td>Open loop gain</td>
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<tr>
<td>$A$</td>
<td>Projected area of the particle in the solution</td>
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<tr>
<td>$C_{ox}$</td>
<td>Gate oxide capacitance</td>
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<tr>
<td>$C_r$</td>
<td>Drag coefficient</td>
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<td>$C_f$</td>
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<td>$C_n$</td>
<td>Nanopore capacitance</td>
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<tr>
<td>$e_{roi}$</td>
<td>Resistor noise referred at output</td>
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<tr>
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<td>Reistor noise referred at input</td>
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<tr>
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<td>$e_{ni}$</td>
<td>Amplifier noise current source</td>
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<tr>
<td>$e_{noi}$</td>
<td>Amplifier current noise at output</td>
</tr>
<tr>
<td>$e_{nv}$</td>
<td>Voltage noise of op-amp</td>
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<tr>
<td>$e_{nov}$</td>
<td>Voltage noise of op-amp at output</td>
</tr>
<tr>
<td>$\epsilon_o$</td>
<td>Permittivity of vacuuum</td>
</tr>
<tr>
<td>$\epsilon_r$</td>
<td>Relative permittivity</td>
</tr>
<tr>
<td>$f_{limit}$</td>
<td>Bandlimit frequency of external filter</td>
</tr>
<tr>
<td>$f_{3db}$</td>
<td>3 dB bandwidth</td>
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<tr>
<td>$g_m$</td>
<td>Transconductance</td>
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<td>Current noise of op-amp</td>
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<td>$I_{nBB}$</td>
<td>Input bias current</td>
</tr>
<tr>
<td>$I_{in}$</td>
<td>Input current</td>
</tr>
<tr>
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<td>Pottasium chloride</td>
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<tr>
<td>$K$</td>
<td>device constant</td>
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<tr>
<td>$\mu_1$</td>
<td>Viscosity of the salt solution.</td>
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<tr>
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<tr>
<td>$\omega_p$</td>
<td>First dominant pole in the transfer function</td>
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<tr>
<td>$R_f$</td>
<td>Feedback resistance</td>
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<tr>
<td>$SNR$</td>
<td>Signal to noise ratio</td>
</tr>
<tr>
<td>$T$</td>
<td>Temperature</td>
</tr>
<tr>
<td>$UGF$</td>
<td>Unity gain frequency</td>
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<tr>
<td>$V_{out}$</td>
<td>Output voltage</td>
</tr>
<tr>
<td>$Z_T(f)$</td>
<td>Transimpedance gain as a function of frequency</td>
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CHAPTER 1

Introduction

1.1 Background

In 1996, a new tool for DNA characterization was proposed where single molecules were forced to pass through a nanopore immersed in an aqueous solution [1]. If a single strand of DNA could be transferred through a nanopore, in the same way as a length of thread is passed through the eye of a needle, it would serve as a device to read off the DNA sequence, which is of interest for genomic applications. Such a system is shown in figure 1.1. This figure shows a nanopore device immersed in an ionic solution. A voltage applied across the device forces single strand of DNA to pass through the nanopore and the resulting current perturbations are fed into the inverting terminal of a transimpedance amplifier to produce a voltage signal. The signal processing block is used to further analyze the voltage pulses.

Initial work in this area was performed using proteinacious nanopores [2, 3, 4, 5]. Although proteinacious nanopores are convenient DNA characterization tools due to their size (2nm diameter), they have shortcomings because of their poor stability and noise. In recent years, artificial solid-state nanopores made of silicon and silicon-containing compounds have begun to replace the original bio-nanopores and promise to overcome the limitations of the latter [6]. The solid-state nanopores can be made with diameters ranging from 1 nm to 100 nm and with a high degree of accuracy.

Before particles, molecules or single strands of DNA can be sent through the nanopore and be identified, the electrical properties of the nanopore must be determined. Moreover the specifications of the amplifier needed to convert the current signal from the nanopore to a voltage depends upon the electrical characteristics of the nanopore.
Figure 1.1: A nanopore-based DNA sequencer. DNA is passed through a nanopore filled with an aqueous solution and the electrical signatures or pulses are amplified using a transimpedance amplifier whose output is further analyzed for the detection of individual nucleotides.

1.2 Purpose of the Research

Most of the literature on transimpedance amplifier design deals with either a high-gain amplifier (120dBΩ–140dBΩ) with bandwidth in the KHz range [7] [8] or amplifiers with high bandwidth (1MHz–100MHz) but a gain of only 50dBΩ–60dBΩ [9] [10]. This work focuses on achieving a transimpedance gain of 120dBΩ and a bandwidth $\geq$ 1MHz.

This research experimentally measured the I-V characteristics and the resistance of a solid-state nanopore device immersed in a 1M aqueous solution of KCl. The capacitance of the nanopore device is determined theoretically.
1.3 Thesis Organization

Chapter 1 introduces the research background and problems being addressed.

Chapter 2 discusses the structure of the nanopore device and the electrical characterization of the nanopore. The experimental results for the resistance of the nanopore and the theoretical result for the capacitance of the nanopore are given. A circuit model for the nanopore device is presented.

Chapter 3 discusses the theory and the design of a low-noise transimpedance amplifier capable of amplifying the signals from the solid-state nanopore device.

Chapter 4 shows the simulation results for the transimpedance amplifier. Two versions of a design with different layouts are presented.

Chapter 5 summarizes this work and suggestions for future work are provided.
CHAPTER 2

Nanopore Device Structure and Characterization

This chapter discusses the physical structure and the electrical characterization of the solid-state nanopore. The resistance of the nanopore is experimentally measured. The capacitance of the nanopore is calculated theoretically.

2.1 Structure of the Solid-State Nanopore

The solid state nanopore devices provided by B. Gierhart [11] were fabricated in a free-standing silicon nitride membrane with a thickness of 30nm-50nm. The nanopore diameter was between 7nm-60nm. The complete structure and the process used to fabricate the device is explained in detail in [11]. Figure 2.1 shows the cross-sectional structure of the nanopore device. The silicon was removed by wet anisotropic etching to form a free standing silicon nitride membrane which produces the 54.7° tapered silicon sidewall. The nanopore is formed in this membrane using high energy electron beam. Transmission electron microscope (TEM) images of three typical nanopores are shown in figure 2.2; the average diameters of the nanopores from left to right are 3nm, 4.5nm and 11.4nm. The nanopores have an irregular shape, but are assumed to be circular in this work to simplify the analysis.

2.2 Nanopore I-V Measurements

Current–voltage measurements are made on devices which have a solid silicon nitride membrane as well as devices that have a nanopore in the silicon nitride membrane. The devices with a solid membrane do not have a nanopore in them. Measurements for these devices are used to determine the maximum operating voltage which
Figure 2.1: Cross-section of the nanopore device. The silicon nitride membrane is nominally 10-30nm and the nanopore diameter ranges from 7nm-60nm. The thickness of the silicone rubber coating is greater than 1mm and is used to reduce the capacitance and the leakage.

Figure 2.2: Typical images of three nanopores. The nanopores have an irregular shape, but are assumed to be circular in this work to simplify the analysis. The average diameters of the nanopores from left to right are 3nm, 4.5nm and 11.4nm. These images are taken from [11].
Figure 2.3: Block diagram showing the experimental setup to measure the resistance of the nanopore.

...can be applied across the dielectric silicon nitride membrane before breakdown. Measurements were repeated on different days and under light and dark conditions.

### 2.2.1 Experimental Setup

A block diagram of the experimental setup to determine the I-V characteristics of a nanopore device is shown in the figure 2.3. A photograph of the experimental setup is shown in figure 2.4. The experimental setup consists of a Ag/AgCl/KCl Microelectrode Half-Cell holder, (World Precision Instruments Inc, model number MEH2S10) into which a 1mm outside diameter capillary is attached. This can be seen on the top right hand corner of the figure 2.4. One end of the capillary is drawn to the order of few micrometers using vertical pipette puller (World Precision Instruments Inc, model number PUL-100) for better control of the tip near the membrane of the nanopore device as shown in figure 2.5. A silicone rubber tube is attached to the half cell holder and used to fill the capillary with a 1M KCl solution. The half cell holder contains an Ag/AgCl termination which serves as the first electrode. The alligator clip on the right hand corner...
Figure 2.4: Photograph showing the setup to measure the I-V characteristics of the nanopore.

Figure 2.5: Photograph showing a closeup of the microtube positioned in the well of the nanopore device. The well is approximately 40 µm on a side at the top of the silicon.
in figure 2.4 connects the electrode to the source measure unit. A 3D micromanipulator not shown in the figure, holds the microtube and allows it to be positioned above the nanopore.

The nanopore device is placed on the agarose [12] gel. This is made of 1M KCl solution containing 1% agarose by weight and can be seen in figure 2.5. A chlorodized Ag strip is used to make the second electrical connection and can be seen attached to an alligator clip in figure 2.4.

To ensure that there is no leakage current around the nanopore device, the backside of the silicon device is coated with silicone rubber (Dow Corning, 734 Flowable Sealant) with a thickness $\geq 1$mm. The silicone rubber extends from the edge of the device to within a radius of 20$\mu$m from the nanopore. The entire setup, excluding the source measure unit, is enclosed in a moisture controlled environment to minimize the evaporation of the aqueous solution from the well of the device. A microscope was placed above the device to accurately position the microtube and monitor the progress of the experiment while it was running. The microscope can be seen at the top in figure 2.4. A photograph taken through the microscope is shown in figure 2.5. This shows a closeup of the microtube positioned in the well of the nanopore device.

The two electrodes are connected to a Keithley 236 source measure unit which can source voltage from 0-10V and measure current on the order of a few hundred pico-amps. The current was measured as the voltage is swept from -0.5V to +0.5V with increments of 0.01V. There was a delay of one second between successive steps. The entire process was automated by a labview program which controls the source measure unit. Working with the nanopore was not easy because the silicon nitride membranes were very delicate and can break easily.
2.2.2 Experimental results on devices with a solid membrane

Figure 2.6 shows the measured I-V characteristics of devices without a nanopore. These devices have a membrane thickness of 30nm. The voltage is swept from -1V to +1V. Six sweeps are taken for each of the devices named alpha and beta. Figure 2.6 shows that the devices without a nanopore have a sinh function and can be approximated to a linear curve for low voltages ($\leq \pm 0.5V$). The resistance of both devices is $>10G\Omega$ in the linear regime. When the voltage exceeds 0.5V, corresponding to an electric field strength of $1.7 \times 10^5$ V/cm the silicon nitride dielectric is no longer in a linear region.

2.2.3 Experimental results on devices with a nanopore

Figure 2.7 shows the I-V characteristics of a nanopore device with a nanopore diameter of 60nm and a silicon nitride membrane thickness of 30nm. The voltage is swept from -0.5V to +0.5V. Ten sweeps are taken with the microtube as the positive terminal (figure 2.7 a)) and with the microtube as the negative terminal (figure 2.7 b)). The I-V curves are linear and from the graphs the resistance of the nanopore is measured to be $4M\Omega$. The resistance of the microtube was measured to be $1M\Omega$. Hence the nanopore resistance is $3M\Omega$. The offset at zero voltage is caused by partial evaporation of liquid in the agarose gel which produces a difference in the chemical potential between the two electrodes.

Figure 2.8 shows the I-V characteristics of a nanopore device with a nanopore diameter of 7nm and a silicon nitride membrane thickness of 30nm. Six sweeps are taken as the voltage sweep is swept from -0.5 to +0.5V. The microtube is the positive terminal in figure 2.8 a) and negative in figure 2.8 b). The measured resistance of the nanopore is $140M\Omega$. No significant changes were observed in the magnitude of ionic current when the setup was run in the dark and in light.
Figure 2.6: Measured I-V characteristics of two devices which do not have a nanopore. The curves are non-linear outside the range of ±0.5V. The resistance is > 10GΩ when the voltage < ±0.5.
Figure 2.7: Measured I-V characteristics for a nanopore device with a diameter of 60nm. The resistance is calculated to be 4MΩ from both the graphs. The resistance of the microtube (1MΩ) needs to be subtracted from this value giving a nanopore resistance of 3MΩ. In a) the microtube is the positive terminal and in b) it is the negative terminal.
Figure 2.8: Measured I-V characteristics for a nanopore device with a diameter of 7nm. The resistance of the nanopore device is approximately 140MΩ. In a) the microtube is the negative terminal and in b) it is the positive terminal.
2.3 Resistance Variation

When a voltage of 0.5V is applied across a nanopore device with a nanopore diameter 7nm having a resistance of 140MΩ, the current through the nanopore is 3.5nA. When nano-sized particles pass through the nanopore, the resistance of the nanopore increases because the path for ionic conduction is partly blocked and would result in a decrease in current. For this work a 10% change in current is specified as the minimum current that is to be detected. This corresponds to 0.3nA. From a previous work [13] on blocking current simulations, we estimate the decrease in current to be on the order of a few hundred pico-amps. From these two results, we conclude that the transimpedance amplifier needs to have sufficient gain to detect current change in the range of 300pA–1nA.

2.4 Capacitance Calculations

There is a capacitance associated with the nanopore device since there is a voltage potential applied across a dielectric membrane of silicon nitride and the silicon. The silicone rubber coating in figure 2.1 extends all the way from the edge of the device to the edge of section 1. Because of this thick insulator on the bottom of the device, the capacitance of the device is dominated by the free standing silicon nitride membrane designated as section 1 in figure 2.1.

Section 1 in figure 2.1 can be taken as a parallel plate capacitor and will have a capacitance given by:

\[ C_1 = \frac{\varepsilon_o \times \varepsilon_{rsn} \times \pi \times (r_1^2 - r_n^2)}{t_n} \]  

(2.1)
where $\epsilon_o$ is the permittivity of vacuum, $\epsilon_{rsn} = 7$, is the relative permittivity of silicon nitride, $r_1$ is the radius of section 1, $t_n$ is the thickness of the silicon nitride membrane and $r_n$ is the radius of the nanopore.

A nanopore device that was studied in this work had a diameter of 7nm and a silicon nitride membrane thickness of 30nm. From equation 2.1 the capacitance of this device is expected to be 2.59pF. A capacitance value of 3pF is used in chapter 3 for the design of the transimpedance amplifier. To minimize device capacitance, the radius of silicon nitride (section 1) should be made as small as possible.

### 2.5 Transit Time

The transit time is defined as the time taken for a charged nano-sized particle to transit through the nanopore under the effect of an electric field. The frequency response of the nanopore device is directly related to the inverse of this transit time. The transimpedance amplifier must be capable of responding in this frequency range. From previous work by Gierhart [11] the transit time for a gold particle passing through a nanopore was measured to be close to $6\mu s$. From another work by Meller [3] and Dekker [6], a transit time for $1\mu s$ per DNA base is specified. In this work, a transit time of $1\mu s$ is used. This relates to a maximum frequency response of 1MHz. This result is used to set the specification of the bandwidth of the transimpedance amplifier designed in chapter 3.
Figure 2.9: Model and cross-sectional diagram of a nanopore device with a variable resistance $R_n$, capacitance $C_n$ and voltage applied to the device $V_n$. Connection of this model to the amplifier is shown in figure 3.2.

### 2.6 Circuit Model of the Nanopore Device

A solid-state nanopore device described above can be modeled with the circuit shown in figure 2.9. The variable resistance $R_n$ represents the modulation of the resistance which occurs when a particle passes through the nanopore, $V_n$ is the voltage across the nanopore and $C_n$ is the associated capacitance. For a device with a 30nm silicon nitride membrane and nanopore diameter of 7nm, the resistor $R_n$ has a value between $140\text{M}\Omega$ and $200\text{M}\Omega$ and the capacitor $C_n$ has a value of 3pF.
CHAPTER 3
Transimpedance Amplifier (TIA) Design

3.1 Introduction

The change in current produced when a particle passes through a nanopore is expected to be on the order of a few hundred pico-amps to a few nano-amps. A transimpedance amplifier (TIA) is needed to convert the current pulse to a voltage pulse. A high-gain ($\geq 1\text{M}\Omega$) and high-bandwidth ($\geq 1\text{MHz}$) amplifier is needed to detect the current pulse from the nanopore. The amplifier also needs to have low noise because the change in current that is being amplified has a low magnitude ($\sim 1\text{nA}$). The bandwidth mentioned above is the transimpedance bandwidth which is also called the closed loop 3dB frequency. This is not the same as the unity gain bandwidth (UGF).

Commercially available amplifiers, such as the Texas instrument’s OPA 657, have a UGF as high as 1.6 GHz [14] but the high input capacitance of 5.7pF of the amplifier adds to the 3pF capacitance of the nanopore, and causes noise gain peaking to occur at 18KHz for closed loop gain of 1M$\Omega$. A low noise operational amplifier designed by Zhu [15] has a UGF of 240MHz with a 20pF load but only has a transimpedance bandwidth of 200–300KHz. Commercially available op-amps that have low input referred noise suffer from high input bias currents of tens of nano-amps such as analog devices AD8599 [16] or have high input capacitance of several pico-farad such as Texas Instruments OPA657 and are not ideal for this application.

3.2 Transimpedance Amplifier Overview

The primary function of a TIA is to convert the current, such as that produced by the nanopore into a voltage, while adding as little noise to the output signal as possible.
Figure 3.1: Simple amplification of a current signal using a resistor.

The amplifier circuit is characterized by several properties including transimpedance gain, 3-db bandwidth, input capacitance and input referred noise voltage.

The transimpedance gain $|Z_T(f)|$ as a function of frequency is the ratio of the output voltage of the amplifier to the input current, and is given by:

$$|Z_T(f)| = \left| \frac{V_{out}}{I_{in}} \right|$$

(3.1)

where $V_{out}$ is the output voltage and $I_{in}$ is the input current.

The most basic TIA configuration is shown in figure 3.1, where the TIA is simply a resistor with a value, $R_L$. The nanopore is replaced with an equivalent circuit model shown in figure 2.9, consisting of an ideal voltage source, nanopore resistance and a nanopore capacitance. Due to variation in the value of resistor $R_n$, current $I_n$ will be produced. This nanopore current passes through the resistor $R_L$ and is converted to a voltage $V_{out}$. The transimpedance gain is equal to the value of the load resistance $R_L$ since all of the nanopore current passes through it. One problem with this simple circuit is that it has a fixed trade off between gain, bandwidth and noise. The transimpedance gain is equal to the value of $R_L$. However, the bandwidth is determined by the RC time constant formed between $R_L$ and the nanopore capacitance $C_n$ [17]. The 3 dB bandwidth ($f_{3dB}$) of the circuit is given by:
\[ f_{3dB} = \frac{1}{2 \times \pi \times R_L \times C_n} \]  

Equation 3.2 shows that for a fixed nanopore capacitance \( C_n \), the resistor \( R_L \) determines the bandwidth. To achieve a large bandwidth, the resistor \( R_L \) needs to be reduced, which reduces the transimpedance gain. Unfortunately the input referred noise current is also dependent on the value of \( R_L \). The noise from the resistor is directly referred to the input such that the mean squared input referred noise current spectral density \( R_{\text{noise}}^2 \) is given by:

\[ R_{\text{noise}}^2 = \frac{4 \times k \times T}{R_L} \]  

where \( k \) is the Boltzmann constant and \( T \) is the temperature in Kelvin. This current noise is directly referred to the input and the noise increases as the resistance decreases.

### 3.3 Transimpedance Amplifier Analysis

Figure 3.2 shows a schematic of a closed loop transimpedance amplifier in which \( I_{\text{in}} \) and \( C_n \) represent the nanopore and its associated capacitance, \( R_f \) is the transimpedance gain resistor or feedback resistor and A represents an ideal operational amplifier. This section deals with deriving the relationship between the unity gain frequency (UGF) of the op-amp and the 3dB frequency of the closed loop amplifier.

From figure 3.2, using nodal analysis on the negative terminal of the op-amp we find:

\[ I_n = \frac{V_1 - V_0}{R_f} + V_1 s C_n \]  

where \( V_1 \) is the voltage at the negative terminal of the amplifier and \( s = j \omega \) in the frequency domain where \( \omega \) is the radian frequency, and the output voltage is \( V_0 \). The
resistor $R_n$ does not affect the analysis if $R_n \gg R_f$ which is true in this case. The output voltage given by:

$$V_0 = \frac{A_0(-V_1)}{1 + s/\omega_p}$$  \hfill (3.5)

where $A_o$ is the open loop gain and $\omega_p$ is the closed loop 3dB pole in radians.

Using equation 3.4 and equation 3.5, the output voltage $V_0$ can be written in terms of $I_n$ after simplifying as:

$$V_0 = -\frac{I_n R_f}{\omega_p A_0} (1 + sC_n R_f)^{-1} + 1$$  \hfill (3.6)

From the above equation, the transimpedance gain is given by $-R_f/D$ where $D$ simplifies to the following:

$$D = \frac{s^2 C_n R_f}{\omega_p A_0} + \frac{s}{\omega_p A_0} + 1$$  \hfill (3.7)

This is a 2nd order equation. The poles of the transfer function are:

$$f_p = \sqrt{\frac{f_c}{2\pi R_f C}}$$  \hfill (3.8)
where \( f_p \) is the 3dB bandwidth, and \( f_c \)

\[
f_c = \frac{\omega_p A_0}{2\pi}
\]

(3.9)

which is the unity gain frequency of the amplifier.

The 3dB bandwidth in equation 3.8 is greater than the 3dB bandwidth in equation 3.2 by a factor of \( \sqrt{2\pi f_c R_f C n} \).

### 3.4 Noise vs Bandwidth Trade–Offs

For the amplification of a current signal on the order of a few hundred picoamps or a few nanoamps, a very high transimpedance gain on the order of \( 1 \text{M}\Omega \) is required. This transimpedance gain is proportional to the feedback resistor \( R_f \), but this resistor contributes to the noise (equation 3.3). A transimpedance gain of \( 1 \text{M}\Omega \) has a resistive current noise of \( 0.128\text{pA/}\sqrt{\text{Hz}} \). To find the total noise that this resistor contributes, we have to integrate the noise density over the frequency range in which the amplifier operates. For example, if we assume a 1MHz bandwidth, the total noise is \( 0.128\text{nA} \). This result is very interesting because it specifies the minimum current that can be detected by an amplifier which uses a resistor as an amplification device. Higher resistor values produce less noise but will provide us with less bandwidth as can be seen from equation 3.8 which leads us to the typical trade off between noise and bandwidth.

It has to be noted that the noise of the amplifier adds to the noise of the resistor. For a well designed amplifier, the amplifier noise is usually 20% - 30% of the noise from the resistor.

A previous amplifier designed by Zhu [15] has a noise of \( 1.28\text{nV/}\sqrt{\text{Hz}} \), which is lower than most of the available commercial amplifiers. But the op-amp has a drawback in terms of its bandwidth capabilities. It has a unity gain frequency of 240MHz which
only produces a 3dB bandwidth in the few hundred KHz range for high transimpedance gain purposes.

### 3.5 High-Gain High-Bandwidth Low-Noise Amplifier Design

The operational amplifier described below was designed using the 240nm IBM BiCMOS 8HP process and a single supply voltage (Vdd) of 2.5V. For designing the amplifier the input capacitance, is assumed to be 3pF based on the calculations presented in Chapter 2 for a nanopore device with membrane thickness of 30nm. The design goal for the 3dB bandwidth of the amplifier is $\geq 1$MHz. As the transimpedance bandwidth is directly related to the $f_c$ of the amplifier from equation 3.8, we need an $f_c$ greater than 1 GHz to achieve a $1M\Omega$ transimpedance gain and a 3dB bandwidth in the MHz range with a 3pF input capacitance.

For low noise amplifiers, the gain of the 1st stage should be much greater than the gain of the subsequent stages. This makes the noise contribution of all the other stages insignificant to the 1st stage. Figure 3.3 shows the schematic of the first two stages of the operational amplifier. The first stage is a cascode stage to provide a high gain. The second stage is npn BJT rather than a FET. This is because a BJT offers higher transconductance with low parasitic capacitance. This helps to push its parasitic pole to a high frequency ($\gg 5$GHz). To achieve a high $f_c$ for the open-loop amplifier, the 1st non-dominant pole is cancelled using the zero nulling resistor method as described in [18]. This strategy cannot be used when the load on the 2nd stage varies. Hence we use a buffer stage in figure 3.4 for the third stage which serves as a constant load for the second stage.

The 3rd stage serves two purposes. First, it loads the 2nd stage with a low capacitive, non-variable load for stability. Secondly, it drives the 20pF instrumental load which the amplifier has to drive for further signal processing requirements. The buffer is not connected in the feedback loop of the transimpedance amplifier. Hence this
Figure 3.3: Schematic of the first two stages of the Op-Amp. The input cascode stage helps to achieve high gain. The second stage uses a npn BJT as an input.
stage does not degrade the stability as long as its pole has a higher frequency than the bandwidth of the transimpedance amplifier. The resistor \( R_e \) is used for biasing the stage. The emitter area of the transistor Mne for the 3rd stage is \(10 \mu m \times 0.12 \mu m\) and the value of \( R_e \) is 890\(\Omega\). This stage also uses a BJT because it provides a high transconductance with low capacitance which helps to push its pole to a high frequency (\(\gg 10\text{MHz}\)).

The design achieves a \( f_c \) of 2.12GHz. The phase margin of this amplifier at the \( f_c \) is actually -25\(^0\). But we do not have to worry about this because the amplifier will only be operating around a few MHz when connected in feedback as a transimpedance amplifier. \( R_z \) in figure 3.3 is the zero nulling resistor and \( C_c \) is the compensating capacitor. The width and length of transistors Mn1 and Mn2 are maximized to produce a low DC offset and low noise. Resistor \( R_b \) is necessary to bias the stage and capacitor \( C_b \) is needed for bypassing \( R_b \) at higher frequencies to obtain gain for this stage. It has a value of 1\(\mu F\) and is external to the chip. Table 4.1 shows the aspect ratios of the transistors and the values of the capacitors and the resistors in the first two stages of the amplifier. The device names are the same as in figure 3.3. Values were optimized by simulation and results are presented in section 3.6.
<table>
<thead>
<tr>
<th>Device</th>
<th>W/L(µm)</th>
<th>Device</th>
<th>W/L(µm)</th>
<th>Device</th>
<th>W/L(µm)</th>
<th>Device</th>
<th>value</th>
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</thead>
<tbody>
<tr>
<td>Mn1</td>
<td>200/0.96</td>
<td>Mp1</td>
<td>60/0.46</td>
<td>Mt</td>
<td>16.41/1.92</td>
<td>R_e</td>
<td>3kΩ</td>
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<tr>
<td>Mn2</td>
<td>200/0.96</td>
<td>Mp2</td>
<td>60/0.46</td>
<td>Mp5</td>
<td>17.4/0.24</td>
<td>R_b</td>
<td>4kΩ</td>
</tr>
<tr>
<td>Mn3</td>
<td>30/0.46</td>
<td>Mp3</td>
<td>75/0.24</td>
<td>Mn5</td>
<td>0.12/2.5</td>
<td>C_b</td>
<td>1µF</td>
</tr>
<tr>
<td>Mn4</td>
<td>30/0.46</td>
<td>Mp4</td>
<td>75/0.24</td>
<td>Mne</td>
<td>0.12/10</td>
<td>R_e</td>
<td>890Ω</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>C_C</td>
<td>40fFΩ</td>
</tr>
</tbody>
</table>

Table 3.1: Aspect ratios and values of various devices in the amplifier. The names for the devices are the same as in figure 3.3 and figure 3.4. For transistors Mne and Mn5, W/L is the emitter width and emitter length.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Parameter</th>
<th>Value</th>
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</thead>
<tbody>
<tr>
<td>Vbp</td>
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<td>Vb2</td>
<td>1.7V</td>
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<tr>
<td>Vbn</td>
<td>2.05V</td>
<td>I_{1ststage}</td>
<td>769µA</td>
</tr>
<tr>
<td>V-</td>
<td>1.6V</td>
<td>I_{2ndstage}</td>
<td>198µA</td>
</tr>
<tr>
<td>V+</td>
<td>1.6V</td>
<td>I_{3rdstage}</td>
<td>882µA</td>
</tr>
<tr>
<td>Vt</td>
<td>1.5V</td>
<td>–</td>
<td>–</td>
</tr>
</tbody>
</table>

Table 3.2: Bias voltages and bias currents for the amplifier. The names for the parameters are the same as in figure 3.3.

### 3.6 Bias Circuit

The bias network for the amplifier, shown in figure 3.5, is an important component for the low noise design. The advantage of this bias circuit is that the currents run through Mp1, Mp2 are insensitive to the supply voltage to first order. A combination of current and voltage routing techniques [19] is used to reduce the mismatch and supply resistance. The transistor’s Mn1, Mn2, Mn3 consist of start-up circuit. Cascode stages are implemented to increase the output resistance of the bias circuit. Table 3.1 shows the aspect ratios of all the transistors in the bias circuit. The device names are the same as in figure 3.5. Table 3.2 shows the bias values and the bias currents for the three stages of the amplifier. The parameter names are the same as in figure 3.3. \( I_{1ststage}, I_{2ndstage}, I_{3rdstage} \) are bias currents in the 1st, 2nd and 3rd stages respectively.
Figure 3.5: Bias circuit for the Op-Amp with its start up circuit.

Table 3.3: Device parameters in the bias circuit. The device names are the same as in figure 3.5. The value of resistor R in the bias circuit is $590\,\Omega$. 
3.7 Amplifier Noise Analysis

The total noise from the amplifier is given by the noise in the cascode stage, the second gain stage, and that of the combination of these two stages with the feedback resistor. The effects of noise gain peaking is included in the analysis.

3.7.1 Noise in the Cascode Stage

To find the noise contributed by the cascode stage figure 3.3, we have to individually find the noise contribution of each mosfet in the stage. The analysis is straightforward and can be found in numerous texts [17] [18] [19] [20]. The noise contributed by the cascode current devices are negligible due to source degeneration effect on them. Hence the major contributors to the noise are the NMOS input pair Mn1 and Mn2 and the PMOS pair of Mp1 and Mp2.

The flicker voltage noise as a function of frequency $f$ is given by:

$$V_g^2(f) = \frac{K}{WLC_{ox}f}$$  \hspace{1cm} (3.10)

where the constant $K$ is dependent on device characteristics and can vary widely for different devices in the same process. The variable $W$, $L$ and $C_{ox}$ represent the transistor’s width, length, and gate capacitance per unit area respectively. Thermal noise is caused by current flowing through a channel and is given by:

$$I_d^2 = 4kT \left(\frac{2}{3}\right) g_m$$  \hspace{1cm} (3.11)

where $g_m$ is the transistors transconductance. This noise from each mosfet is directly referred to the input for the four transistors Mn1, Mn2, Mp1 and Mp2.
3.7.2 Noise of the Second Gain Stage

The voltage noise contributed by the BJT \cite{20} is given by:

\[ V_i^2 = -4kT \left( r_b + \frac{1}{2g_m} \right) \]  \hspace{1cm} (3.12)

where \( r_b \) is due to the thermal noise in the base resistance and the term \( \frac{1}{2g_m} \) is due to the collector shot noise.

The current noise \cite{20} is given by:

\[ I^2(f) = 2q \left( I_B + \frac{K_d I_B}{f} + \frac{I_c}{\beta(f)^2} \right) \]  \hspace{1cm} (3.13)

where \( 2qI_B \) is a result of base current shot noise, \( K_d I_B / f \) models the \( 1/f \) noise (\( K_d \) is a constant that depends upon device properties) and \( I_c \) is the input-referred current shot noise and \( \beta_f \) is the current gain.

This noise of the PMOS transistor calculated by equation 3.11 is added to equation 3.13 to obtain the total noise. Both these noises are directly referred to the input of the 2nd stage and they should be divided by the gain of the 1st stage to find the 2nd stage’s contribution to the total input referred noise.

3.7.3 Noise Analysis of the Transimpedance Op-Amp

The total noise when the op-amp is used as an transimpedance amplifier requires further computations because the contributions of the voltage noise, current noise and resistor noise together with the noise gain peaking caused by the input capacitance of the nanopore have to be considered here. Below the noise contribution from each of these sources is considered.
3.7.3.1 Resistor Contribution

Resistor $R_f$ contributes a voltage noise of $\sqrt{4kTR_f}$ which is referred directly to the output as can be seen from the figure 3.6. This can also be represented as a current source (figure 3.7) of $\sqrt{4kT/R_f}$ which in this case is directly referred to the input and its contribution at the output would be this value multiplied by $R_f$ (the transimpedance gain). It can be seen that the noise can be represented by either a voltage source or a current source but not both. They both have the same effect on the output and the signal to noise ratio (SNR) decreases as the value of the resistor increases by the ratio $\sqrt{R}$. The noise at the output of the amplifier is given by:

$$e_{roi}^2 = e_{ri}^2 \times R_f^2 = 4kTR_f$$

(3.14)

where $e_{roi}$ is the resistor noise referred at output of the amplifier, $e_{ri}$ is the resistor noise referred at input of the amplifier.
3.7.3.2 Current Noise Contribution from the Amplifier

Current noise produced by the amplifier is shown in figure 3.8 [20]. The noise gain for this current source is the same as the transfer function of the transimpedance amplifier. The value of the current noise for a MOS input is on the order of a few femtoamps and is usually negligible compared to the other sources of noise. Its noise nevertheless at the output is given by:

\[ e_{nio}^2 = i_{ni}^2 \times R_f^2 \]  \hspace{1cm} (3.15)

where \( e_{nio} \) is the voltage at output due to input noise current \( i_{ni} \).

3.7.3.3 Voltage Noise Contribution and Noise Gain Peaking

The voltage noise source for the amplifier is shown in figure 3.9. The noise source is connected to the non-inverting input by definition [21] [22]. To find the contribution of this noise source we have to find the noise gain for this source which is not always the same as the signal gain.
Figure 3.8: Current noise model of the op-amp. The current noise in amplifiers using CMOS inputs is very low (on the order of a few femto-amps) as compared to BJT inputs (on the order of a few nano-amps).

Figure 3.9: Voltage noise model of the op-amp. The noise source is placed at the non-inverting terminal of the amplifier by definition.
From the topology it can be seen that the noise gain transfer function $A_n$ is given by:

$$A_n = 1 + sR_fC_{in}$$

(3.16)

and the noise at the output of the amplifier is given by:

$$e_{nov}^2 = e_{nv}^2 \times (1 + sR_fC_{in})^2$$

(3.17)

where $e_{nv}$ is the voltage noise of the op-amp at the input and $e_{nov}$ is the voltage noise of op-amp at output.

From the above equation it can be seen that the magnitude of the transfer function peaks after it encounter its zero. This is called noise gain peaking and it caused by the inherent input capacitance of the nanopore and resulting in a 20db/decade noise increase. The lower the capacitance, the higher the frequency at which noise gain peaking starts.

The Texas Instrument’s OPA 657 has an input capacitance of 5.4pF which when combined with the 3pF of the nanopore adds up to 8.4pF. The design described here has an input capacitance of 250fF which would add to the 3pF capacitance of the nanopore to give a total capacitance of 3.25pF. The lower total capacitance causes the noise gain peaking to occur at a higher frequency and reduces the total noise.

Noise gain peaking is actually a huge problem because it renders the advantage of a high bandwidth useless because as soon as noise gain peaking starts, the noise begins increasing at 20db/decade.

Because the various noise sources are uncorrelated, the equation that gives us the total noise is given by:

$$e_{not} = \sqrt{e_{nio}^2 + e_{roi}^2 + e_{nov}^2}$$

(3.18)
where $e_{not}$ is the total noise at the output. Combining equation 3.14, 3.15, 3.17 and 3.18, the output voltage is given by:

$$e_{not} = \sqrt{i_{ni}^2 R_f^2 + 4kT R_f + e_{nv}^2 \times (1 + sR_f C_{in})^2}$$  

(3.19)

To find out the input referred noise, we shall divide the above equation by the transimpedance gain $R_f$, to obtain:

$$i_{nit} = \sqrt{\frac{i_{ni}^2}{R_f} + \frac{4kT}{R_f} + \frac{e_{nv}^2}{R_f^2} \times (1 + sR_f C_{in})^2}$$  

(3.20)

Equation 3.20 gives the total input referred noise of this amplifier when used as a transimpedance purposes. To find the total noise in a given bandwidth, the total noise is squared and integrated over the bandwidth.

### 3.8 Compensation for Noise Gain Peaking

Due to the 2nd order response of the transimpedance amplifier and the noise gain peaking, it is necessary to compensate the amplifier so that the noise does not increase to abnormally high values.

From the transfer function of the noise gain given by equation 3.16, it can be seen that if there was a pole in the transfer function, it would compensate the effect of the zero and reduce the peaking. This can be achieved by adding a capacitor in parallel with the feedback resistor. The transimpedance amplifier with the phase compensation capacitor is shown in figure 3.10.

The noise gain transfer function now becomes:

$$A_n = \frac{1 + sR_f(C_n + C_f)}{1 + sR_f C_f}$$  

(3.21)
Figure 3.10: Amplifier with phase compensation. The compensation capacitor $C_f$ is used to stabilize the amplifier when its used in feedback. The block A represents the amplifier from figure 3.3. $R_f$ has a value of 1MΩ and $C_f$ has a value of 20fF. $C_n$ is 3pF and $I_n$ represents the current from the nanopore.

where $C_f$ is the feedback compensation capacitor. A judicious choice for $C_f$ causes the pole in the transfer function to compensate for the noise gain peaking. The value of $C_f$ is determined by both stability and noise requirements.

3.9 Improving Closed Loop Stability

A minimum phase margin of 60° near a frequency of 1MHz was chosen for this design to provide good stability. To find the value of $C_f$ which gives us this phase margin, we have to find out the total phase shift of the amplifier that occurs at all frequencies in the desired bandwidth. The total phase shift for this design is the phase shift of the open loop amplifier added to the phase shift of the feedback loop. The feedback loop has a pole at 53KHz. Hence it’s phase shift at all frequencies can be found out. From simulations, the phase shift of the open loop amplifier was determined to be 54° at 2MHz.
Figure 3.11: Closed loop stability test. Figure shows $V_t$ as the test voltage source at the non-inverting terminal of the amplifier. This setup is used to test the phase loop and loop gain of the amplifier. The phase and gain are measured at node X.

The frequency where a total phase shift of $120^\circ$ occurred was determined from simulation. If we do not want the phase to degrade more than $120^\circ$, then it is at this frequency around which a zero should be added to cause a positive phase shift in the feedback path (pole for the noise gain transfer function).

To find the phase shift of the transimpedance amplifier, the feedback loop has to be broken at a suitable point where we can apply a test signal and phase shift determined at the other end of the breakage. It is important that the point where the feedback loop is broken is chosen such that we do not break the feedback path but just the loop [23].

From figure 3.11, it can be seen that the point chosen was at the negative terminal of the op-amp. The advantage of choosing this point is that, when we apply a test voltage source at the negative terminal (which has a high input impedance) we can be sure that the test source is not loaded by the amplifier. The DC bias voltage should remain the same when this simulation is performed.

We calculate the phase shift at point marked X in figure 3.11. The phase shift at this point at any particular frequency is the phase shift of the amplifier added with the
phase shift from the feedback loop. After adding $C_f$ with a value 20fF, the design has a maximum phase shift of $120^\circ$ at a frequency of 1MHz which gives us a phase margin of $60^\circ$. This will ensure the circuit would not be oscillating during feedback. Thus $C_f$ was set at 20fF.
CHAPTER 4
Amplifier Simulation Results

This chapter shows the simulation results for the amplifier when used as a voltage to voltage amplifier and when used in closed loop as a transimpedance amplifier. All simulations results are based on the layout of the amplifier with extracted parasitics. Noise simulation results are shown for two different layouts of the amplifier. In one of the designs, fingers (multiple gates tied in parallel) are used for the input pair Mn1 and Mn2 and the PMOS pair Mp1 and Mp2. This layout shown in figure 4.1 produces a compact design with an area of $118 \mu m \times 149 \mu m$. The second layout shown in figure 4.2 did not incorporate fingers and had an area of $247 \mu m \times 168 \mu m$. Simulation results showed an increase in the input referred noise in the more compact design. This needs to be verified experimentally. All the other AC and DC characteristics were identical in the two layouts. The entire amplifier dissipates a power of 17.7mW.

Figure 4.3, shows the open-loop gain and phase shift vs frequency for the amplifier. The response shows a low frequency zero near 100Hz. This zero is introduced by the combination of $R_b$ and $C_b$ in the second stage shown in figure 3.3 which form a high pass filter. Capacitor $C_b$ is used to negate the effect of degenerating resistor $R_b$. The $f_c$ from the simulation is 2.12GHz. The open-loop phase shift at 1MHz and 5MHz is -42.5° and -80.12° respectively. The open-loop gain is 85dB. Figure 4.4 shows the input referred noise as a function of frequency for the op-amp with and without fingers. The dashed line shows the noise plot when finger are used. The noise at 100KHz, 1MHz and 10MHz is $5.4 nV/\sqrt{Hz}$, $3.5 nV/\sqrt{Hz}$, $3.2 nV/\sqrt{Hz}$ for no fingers and $12.4 nV/\sqrt{Hz}$, $11.2 nV/\sqrt{Hz}$, $11 nV/\sqrt{Hz}$ when fingers are used.

Figure 4.5 shows the closed loop gain when the amplifier is used as a transimpedance amplifier with the feedback resistor $R_f = 1M \Omega$, compensation capacitor $C_f = 20fF$ and nanopore capacitance $C_n = 3pF$. The 3db frequency is 4.1MHz from
Figure 4.1: Layout of the amplifier when fingers are used in the layout. The noise when such a layout is used is more than the noise when no fingers were used. $C_f$ has a value of 20fF and $R_f$ has a value of 1MΩ. It has an area of $118\mu m \times 149\mu m$.

This graph. This is the frequency region which is of interest when operating in feedback. The transimpedance gain is $120\,dB\Omega$. The roll-off is 40dB/decade because of the 2nd order response.

Figure 4.6 shows the loop gain and the loop phase of the amplifier. The loop gain is the gain of the amplifier around its feedback loop and the loop phase of the amplifier is defined as the phase shift of the amplifier around its feedback loop. They are both measured by breaking the feedback loop at a suitable point, injecting a test source at one end and finding the gain and phase at the other end. These results are used to analyze the stability of the amplifier in feedback. The phase margin always stays above $60^\circ$ which means good signal stability and the loop gain reaches zero at a frequency of 300MHz, well before the phase shift reaches $360^\circ$ at frequency of 600MHz. This indicates that the amplifier is stable in the entire range of its operation from 0 to 5MHz.
Figure 4.2: Layout of the amplifier when fingers are not used in the layout. $C_f$ has a value of 20fF and $R_f$ has a value of 1MΩ. It has an area of $247\mu m \times 168\mu m$. 
Figure 4.3: Open-loop gain and phase of the op-amp when used as a voltage to voltage amplifier. The open-loop gain is 85dB and the $f_c$ is 2.12GHz.

Figure 4.4: Input referred noise as a function of frequency for the op-amp with and without fingers. The dashed line shows the noise plot when finger are used. The noise at 100KHz, 1MHz and 10MHz is $5.4\text{nV}/\sqrt{\text{Hz}}$, $3.5\text{nV}/\sqrt{\text{Hz}}$, $3.2\text{nV}/\sqrt{\text{Hz}}$ for no fingers and $12.4\text{nV}/\sqrt{\text{Hz}}$, $11.2\text{nV}/\sqrt{\text{Hz}}$, $11\text{nV}/\sqrt{\text{Hz}}$ when fingers are used.
Figure 4.5: Transimpedance gain of the amplifier in dBΩ vs frequency. The gain is 120dBΩ at DC and the 3dB frequency is 4.1MHz.

Figure 4.6: Loop gain and loop phase of the amplifier when used as a transimpedance amplifier. These results were taken from the analysis described in section 3.9. The phase plot shows a maximum phase shift of 120° from -180° to -300°. Hence the phase margin is 60°.
Figure 4.7 and figure 4.8 show the transimpedance noise plots for the amplifier with and without fingers. The dashed lines show the noise plot when finger are used. Fingers are used on the input pairs.

Figure 4.8 shows the simulated voltage noise in $V/\sqrt{Hz}$ as a function of frequency seen at the output of the amplifier. The gain peaking due to the input capacitance can be seen taking affect at around 600KHz for layout with no fingers. The compensation capacitor levels this peaking at around 7MHz. Additional peaking occurs due to non-dominant poles at higher frequencies but these frequencies lie after the bandwidth of the amplifier and are not of concern. For the layout with fingers noise gain peaking takes affect near 300KHz. There is an increase in noise which is not understood and needs to be verified experimentally.

A comparison of the amplifier designed here with the OPA657 from Texas Instruments and Zhu’s amplifier is shown in table 4.1. The advantages of this design is its higher UGF, lower input capacitance and smaller phase shift at 1MHz which translates into better stability when operated in feedback.
Figure 4.8: Simulated output noise plots for the transimpedance amplifier with and without fingers. The dashed line shows the noise plot when fingers are used. The corner frequency is close 1KHz for both plots. Noise gain peaking starts at 600KHz when fingers are not used as compared to 300KHz when fingers are used in the layout.

Table 4.2 shows the simulation results of the transimpedance amplifier for this design. Results are shown for layout with and without fingers. $f_{\text{limit}}$ is the maximum frequency allowed by an external filter. The total noise is calculated by integrating the current noise density from 0 Hz to $f_{\text{limit}}$. The total noise includes the thermal and the flicker noise components. The amplifier has a $f_{3dB}$ of 4.1MHz. The phase margin always remains above 60°.

<table>
<thead>
<tr>
<th></th>
<th>Zhu</th>
<th>OPA 657</th>
<th>This Design</th>
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<tbody>
<tr>
<td>Open-loop gain</td>
<td>120dB</td>
<td>75dB</td>
<td>75dB</td>
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<tr>
<td>Gain Bandwidth Product $f_c$</td>
<td>240MHz</td>
<td>1.6GHz</td>
<td>2.12GHz</td>
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<tr>
<td>Voltage noise at 1MHz</td>
<td>1.8nV/$\sqrt{\text{Hz}}$</td>
<td>4.8nV/$\sqrt{\text{Hz}}$</td>
<td>3.5nV/$\sqrt{\text{Hz}}$</td>
</tr>
<tr>
<td>Voltage noise at 10MHz</td>
<td>1.8nV/$\sqrt{\text{Hz}}$</td>
<td>4.8nV/$\sqrt{\text{Hz}}$</td>
<td>3.2nV/$\sqrt{\text{Hz}}$</td>
</tr>
<tr>
<td>Phase shift at 1MHz</td>
<td>90°</td>
<td>72°</td>
<td>54°</td>
</tr>
<tr>
<td>Phase shift at 10MHz</td>
<td>95°</td>
<td>89°</td>
<td>90°</td>
</tr>
<tr>
<td>Input capacitance</td>
<td>2pF</td>
<td>5.7pF</td>
<td>250fF</td>
</tr>
</tbody>
</table>

Table 4.1: Comparison of the open-loop amplifier with OPA 657 and Zhineng Zhu’s Op-Amp.
Table 4.2: Summary of simulation results for the transimpedance amplifier. $R_f$ was set to 1MΩ. $f_{\text{limit}}$ is the bandwidth of the external filter. The total noise is calculated by integrating the current noise density over $f_{\text{limit}}$. The amplifiers $f_{3\text{dB}}$ is 4.1MHz. The phase margin always remains above 60°.

<table>
<thead>
<tr>
<th>$f_{\text{limit}}$ (MHz)</th>
<th>R_{\text{noise}} (nA)</th>
<th>Phase Margin at $f_{\text{limit}}$ (deg)</th>
<th>Total noise no fingers (nA)</th>
<th>Total noise with fingers (nA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.13</td>
<td>65</td>
<td>0.16</td>
<td>0.30</td>
</tr>
<tr>
<td>2</td>
<td>0.18</td>
<td>60</td>
<td>0.31</td>
<td>0.70</td>
</tr>
<tr>
<td>3</td>
<td>0.22</td>
<td>62</td>
<td>0.54</td>
<td>1.54</td>
</tr>
<tr>
<td>4</td>
<td>0.25</td>
<td>63</td>
<td>0.74</td>
<td>1.87</td>
</tr>
</tbody>
</table>

4.1 Amplifier Testing

After fabrication is complete the amplifier can be tested by applying a voltage of 2.5V Vdd. The inverting and non-inverting terminal of the amplifier should to be biased at 1.6V. The only external component required is the capacitor $C_b$. Capacitance of 1µF needs to be placed between the pins labeled ’ex_cap’ and ’gnd’ in the layout. To measure the transimpedance characteristics an AC current source can be applied to the inverting terminal and the voltage at the output terminal measured.

4.2 Summary of the Transimpedance Amplifier

A high-gain, high-bandwidth, low noise transimpedance amplifier has been designed using 240nm IBM BICMOS 8HP process. The work has achieved a transimpedance gain of 120dBΩ and a bandwidth of 4.1MHz with a noise of 130fA/$\sqrt{Hz}$ at 1MHz and dissipates a power of 17.7mW. It has to be bandlimited to 1MHz depending upon the magnitude of the input current pulse because noise gain peaking degrades the noise performance of the amplifier after 1MHz. For example, if we are trying to detect a 1nA pulse, the total noise in 1MHz is 0.164nA, hence the amplifier cannot be used beyond 1MHz because the noise itself comes close to 1nA. But it can still detect a current pulse of 2nA or greater. The input referred noise increases from 0.164nA in a 1MHz bandwidth to 0.648nA in a 4.1MHz bandwidth. The compensation feedback capacitor does
not help in this case because if we try to move the noise gain peaking pole to a lower frequency to reduce noise gain peaking, it reduces the bandwidth. This is because of the limited $f_c$ of 2.12GHz of the open loop amplifier. The amplifier is stable with a phase margin of 60° at 2MHz. Two layouts were presented. A more compact design with an area of $1.75 \times 10^4 \mu m^2$ has a higher noise than a larger design with an area of $4.14 \times 10^4 \mu m^2$. The difference is the use of fingers in four transistors in one layout as compared to no fingers in the other one. The amplifier has a low input capacitance of 250fF which helps in controlling the noise gain peaking.
CHAPTER 5
Conclusions and Recommendations for Future Work

This research involved electrically characterizing the I-V response of a solid-state nanopore device and designing a transimpedance amplifier to amplify a current produced when a device produces a current change on the order of a few hundred pico-amps.

The resistance of a nanopore device with a nanopore diameter of 7nm and a silicon nitride membrane thickness of 30nm was measured to be 140MΩ. Such a nanopore device had a non-linear I-V characteristic when a voltage exceeding 0.5V, corresponding to an electric field of $\sim 1.7 \times 10^5$ V/cm, is applied across it. Voltages exceeding 5V or a field of $\sim 1.7 \times 10^6$ V/cm or greater for a short period of time will electrically break down the membrane. The nanopore operates in a linear region in the voltage range from -0.5 to +0.5V. There was no breakdown when 0.5V was applied for a duration of 24 hours.

The transimpedance amplifier, designed in a 240nm IBM BiCMOS process, achieved a total input referred noise of 0.164 nA over a 1MHz bandwidth, a transimpedance gain of 120dBΩ and a low input capacitance of 250fF which helps to reduce the noise caused by noise gain peaking. This amplifier meets the requirements to detect a signal from a nanopore device and is an improvement over commercially available amplifiers such as the OPA657 [14] or the AD8599 [16]. The research has also reviewed an important characteristic of transimpedance amplification called noise gain peaking and has discussed its impact on the noise characteristics of the amplifier.

For future work, the value for the capacitance of the solid state nanopore needs to be experimentally verified as the characteristics of the final pulse observed depends to a large extent on the capacitance. As the input capacitance of the amplifier decreases, noise gain peaking starts at a higher frequency and the bandwidth is improved. The
capacitance of the nanopore device can be minimized by reducing \( r_1 \), the radius of the silicon nitride membrane not covered with silicon shown as section 1 in figure 2.1. If \( r_1 \) can be reduced to 1\( \mu \)m (from its current value of 20\( \mu \)m) and a silicon nitride membrane thickness of 10 nm, then its associated capacitance would just be 60 fF, compared to 3 pF for the current nanopore devices. This change will reduce the total noise by decreasing noise gain peaking and allow the amplifier to operate at higher frequencies.

For future amplifier designs, a recommendation would be to further increase the value of the unity gain bandwidth \( f_c \) of the amplifier using a more advanced microelectronics technology. The noise in the transimpedance amplifier is dominated by the feedback resistor in this amplifier design; future work could involve the use of an active device for amplification which has less spectral noise density than a resistor. Different topologies for amplification could also be considered.

The amplifiers need to be fabricated and the design experimentally verified. The noise produced by the two amplifier layouts needs to be experimentally verified.
REFERENCES


BIOGRAPHY OF THE AUTHOR

Raghu Tumati was born in Madras, India on November 16, 1982. He received his high school education from Kendriya Vidhyalaya in India.

He entered Pune University in 2001 and obtained his Bachelor of Engineering degree in Electrical Engineering in 2005.

In September 2005, he was enrolled for graduate study in Electrical Engineering at The University of Maine and served as a Teaching Assistant and a Graduate Research Assistant. His current research interests include analog and mixed-signal circuit design. He is a member of IEEE, and his interests include playing tennis, cricket, sailing and windsurfing. Raghu is a candidate for the Master of Science degree in Electrical Engineering from The University of Maine in May 2008.