ECE 571 – Advanced Microprocessor-Based Design Lecture 18

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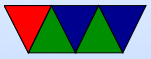
5 April 2018

Announcements

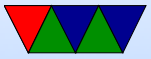
- HW#9 will be posted



Reading of the Article

http://anandtech.com/show/9582/intel-skylake-mobile-desktop-launch-architecture-analysis/

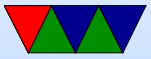
The Intel Skylake Mobile and Desktop Launch, with Architecture Analysis by Ian Cutress



Background on where info comes from

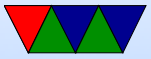
Intel Developer Forum This one was in August 2015

Name	tech		Year
Conroe/Merom	65nm	Tock	2006
Penryn	45nm	Tick	2007
Nehalem	45nm	Tock	2008
Westmere	32nm	Tick	2010
Sandy Bridge	32nm	Tock	2011
Ivy Bridge	22nm	Tick	2012
Haswell	22nm	Tock	2013
Broadwell	14nm	Tick	2014
Skylake	14nm	Tock	2015
Kaby Lake	14nm	Tock	2016
CoffeeLake	14nm	Tock	2017
CannonLake	10nm	Tick	2018
IceLake	10nm+	Tock	2019?

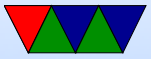


Notes

- Clock: tick-tock. Upgrade the process technology, then revamp the uarch.
- 14nm technology? Finfets?
- What technology are Pis at? 40nm?
- 14nm yields getting better.
- hard to get, even with electron beam lithography
- plasma damage to low-k
- silicon only 0.111nm
- finfet. Intel has plants Arizona, etc.

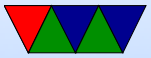


- Delay to 10nm
- 7nm? EUV?

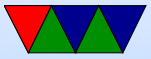


Skylake Processor – Page 1

- "6th generation" – Intel naming is awful
- Confusing naming i3, i5, i7, Xeon, Pentium, m3, m5, m7, etc.
- 4.5W ultra-mobile to 65W desktop
- They release desktop first these days. For example just last year releasing "Xeon E5-2600 v4" AKA Broadwell-EP, and Skylake-SP came out July 2017

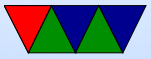


- YUHS – number of cores, level of graphics
- Number of pins important. Low-power stuck with LPDDR3/DDR3L instead of DDR4 possibly due to lack of pins?
- 128M of eDRAM? For GPU?
- Intel no longer releasing info on how many transistors/transistor size? "no longer relevant for the end-user experience?"

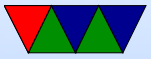


Skylake Processor – Page 2

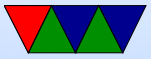
- "mobile first" design. Easier to scale up than down?
- Want to use in tablets. What % of market does intel have on tablets?
- Up to 60% lower active power (win8.1 video playback, i7-6920HQ vs i7-4910MQ)
- Up to 60% faster estimated SPECint 2006 (i5-6300HQ vs i5-4300M)



- Up to 40% better graphics On 3DMARK Sky Diver overall (m76Y75 vs m5Y71)
- Overtook AMD performance on integrated graphics (though costing more)
- Power features:
  - Fine grain power gating (core, system agent, graphics, chipset)
  - Digital PLL
  - HW and Cdyn reduction(?) (cdyn is capacitance)
  - Lower Vmin

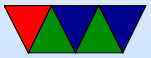


- DDR, Serial I/O power optimization
- Speed shift
- C9 display with Self Refresh Panel
- “modern standby”
- Configurable power management (i.e. the OEMs can customize, it’s off chip again)



Skylake Processor – Page 3

- Microarchitecture
- Lanes increased to 128B between cores
- Sound DSP, faster DDR memory, advanced integrated graphics, wider core, enhanced LLC
- DDR3L and DDR4
- 16 PCIe lanes (what is PCI typically used for? external GPUs and disk)
- DMI 3.0 (8.0GT/s, 3.93GB/s), but motherboard traces down to 7in from 8in?

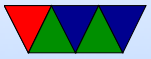


DMI=direct media interface, connection between north and south bridge multiple lanes, differential signaling

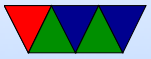
- PCIe can be provided by either CPU or chipset?
- Chipset on package, low power I/O OPIO (on-package I/O) 1pJ/bit
- Haswell/Broadwell had FIVR (fully integrated voltage regulator)

  simpler design, higher temperatures, made overclocking harder

  Z-height problem, too big transistors, holes in motherboard for capacitors and inductors (for tablets

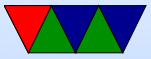


want as flat as possible)

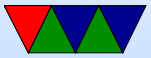


Skylake Processor – Page 4

- New socket, LGA 1151 (soldered use BGA 1515, BGA 1356 and BGA 1440), not back compatible
  expected, intel usually changes socket every two releases
- Intel RST on PCIe storage?
- USB-A vs USB-C, thunderbolt
- DRAM: DDR3L vs DDR4. SO-DIMM
  Note DDR3L is not same as LPDDR3
- Two memory controllers per channel. Max of 4*16GB = 64GB

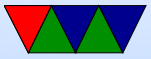


- Memory speed of 15-15-15

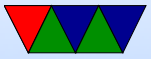


Skylake Processor – Page 5

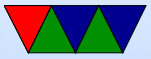
- Performance clock-per-clock only 6% over Haswell and 3% over Broadwell
- Larger instruction window, extract more parallelism
- Can dispatch 6 uops at once (over 4uops for Haswell)
- "Higher-capacity and improved" branch predictor
- "Faster prefetch"
- Shorter latencies
- more units
- Power down when not in use



- Speedup AES-GCM and AES-CBC
- Better branch predictor, no details
- Improved Divider
- FMultiplier regress to Haswell numbers because it allows better performance for enterprise silicon?
- FMUL only disclosed when asked about a rumor?
- Deeper store buffer
- Improved page miss handling (probably mem not tlb?)
- Better L2 cache miss bandwidth
- New instructions for cache management (for NVRAM?)
- Better hyperthreading

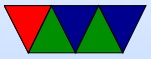


- L2 reduced from 8-way to 4-way. Saves power and area? Similar to Haswell performance with lower power
- Intel sells custom configured silicon if you are a bit enough customer
- Security Tech – SGX software guard extensions? Encrypted memory (why is that a good idea?)
- Intel MPX (memory stack/heap protection)
- Trusted execution, protected enclaves
- eDRAM – embedded DRAM – L4 cache? For graphics card? 64MB and 128MB



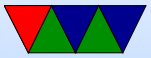
Skylake Processor – Page 6

- Gen9 Graphics
- Multiple graphics sizes, can scale for power on smaller
- Lossless data compression – save power and perf by compressing before sending across bus
- 16-bit float support – less accuracy, lower power
- MPO – multiplane overlay
  can scale and such in the GPU without going back and forth to CPU

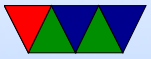


Skylake Processor – Page 7

- Battery Life
- Speed shift
- System Agent
- PCU – power control unit, possibly even embedded intel CPU RAPL?
- Up to 4 independent power domains
- High granularity power gating, at least 12 gates
- Several frequency domains: core, uncore, 2 GPU, eDRAM

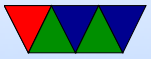


- Intel Speed Shift – let CPU control power, rather than the OS. OS can take up to 30ms to adjust, chip can do it in 1ms.
- HAVE CMOS power equation, but say dynamic plus static is approximately f**3
- Psys, knows total system power total power provided to CPU
- Race to Idle
- Diminishing returns. Reintroduce idea of duty cycle (see old p4 implementation)
- Can turn off CPU cores as often as 800us



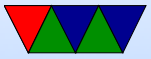
Skylake Processor – Page 8

- Kaby Lake (kah-bee lake)
- 14nm – 90 silicon atoms
- Increasing yield, what does that mean and why important
- Fabs Oregon, Arizona, Ireland

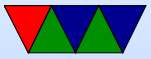


Further Notes

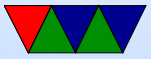
- Kaby Lake
  - October 2016 (laptop) January 2017 (desktop)
  - 14FF++ process
  - Clock frequency increase
  - Some support Optane?
  - Not supported pre-Windows 10
  - Unclear how much speed improvement
- Another break in tick/tock, a 4th 14nm introduced
- Coffee Lake



  - October 2017.
  - 14nm++
  - i3/i5/i7 changes. i3 no hyperthreading?
  - Same socket as Sky/Kaby but electrically incompatible
  - April 2018 release i9 chip?
- Cannon Lake
  - 10nm
  - Supposed to be out in 2016, pushed to 2018
  - In theory some have started shipping?
- Ice Lake
  - 2019?

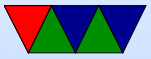


- Has meltdown/spectre fixes?
- 10nm++

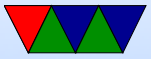


Skylake-SP Article

- https://www.nextplatform.com/2017/07/11/x86-bat
- Xeon Scalable Processor
- Up to 28 cores
- Single Socket P (older E5 and E7 not compatible, buffered vs unbuffered dim)
- Ultra-path interconnect (replace QPI?)
- No Optane support yet
- Four classes: Bronze, Silver, Gold, Platinum
- AVX-512 support

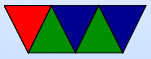


- L2 raised from 256k to 1MB
- RDIMM, LRDIMM? Load Reduced DIMM, buffer both control and data signals



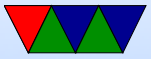
Intel 8th Generation Article

- `https://www.anandtech.com/show/12607/intel-expa`
- Article from just a few days ago
- 8th generation == (7th was Kabylake, 6th Skylake?)
- Intel confusing thing, their 8th gen branding includes Kabylake Kabylake Refresh, and Coffeelake
- Intel announced will be more fluid on naming
- Intel Mobile i9-8950HK with "Thermal Velocity Boost" 6 cores, 12 threads, 4.6GHz turbo boost
- Intel sells intel chips with AMD graphics tacked on (plus



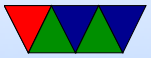
HBM2 memory)

- EDRAM –
- Coffeelake Desktop – i7/i5/i3/Pentium Gold/Celeron
- Optane – until now could only use to speed up boot hard-drive, now can do any hard-drive?



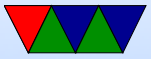
Atom Article

- Good practice using IEEE explore
- Intel Atom C2000 Processor Family: Power-Efficient Datacenter Processing
- From HOTCHIPS. Conference every year, highlights invited to write up paper for IEEE Micro

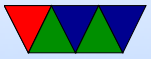


Atom Article p1

- Avoton/Rangely
- Atom is Intel's embedded line, but this one designed to be used in servers
- Why is Intel worried about dense servers using embedded processors?
- Seven times performance and six times power saving than previous? (they mean against the very first atom design S1200 a long time ago)

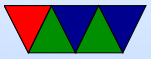


- 22nm tri-gate
- “cold storage” segment?
- Microservers

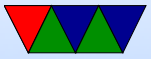


Atom Article p2-3

- Tradeoff single-thread perf for larger threads, higher energy density
- Avoton – 2,4,8 threads, 6-20W, 22nm
- Low leakage power. Takes the "Silvermont Tock"
- Each pair of Silvermont cores 1MB L2 cache
- 25.6GB/s the two channels of DDR3/3L can provide

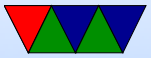


- North Complex, SSA, P-Unit



Atom Article p4-5

- South Complex
- PCH – legacy hardware like i8259, io-apic
- 4 Ethernet ports, at least 1GB. fast, also removes need for additional Ethernet chip on motherboard (saves space and power?)
- PCIe
- SATA drives, USB2

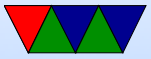


- Why no USB3? not really used on server (kb, mouse, debug)

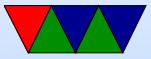
- Rangely – communications segment

- four workloads — application processing, control processing, packet processing, and signal processing
  Rangely can do all but the last (need higher end chip with AVX for that)

- Rangely adds QAT crypto hardware, reliability, warranty guarantees (see recent news on failing Atom chips)



- Fast IP Forwarding



Atom Article p6

- Silvermont
- 35% IPC improvement
- now an out-of-order processor
- 2x better than previous saltwell
- Fig 5: large branch predictor (gshare?), L1 inst prefetch, more single uop, OOO, larger l2 cache, lower l2 latency, faster mul/div/fp-add, larger data TLB, OoO loads, better mem copy perf, better cache miss tolerance