Video RAM

Vince Weaver
ECE699

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Source

Much of the material from this comes from http://www.lostcircuits.com/memory/ddr3/

Background

- Linear vs Random Access
- UMA (Uniform Memory Access)
- 1024x768x16bit@75Hz requires 117.9Mbytes/s

VRAM/WRAM

- Mid 90s
- Dual ported. Special serial interface for screen refresh.
- Some custom improvements, mainly block-fill.
- WRAM similar but sole-source.
- cost 1.7 to 2 times equivelant DRAM.

SGRAM

- Equivelant to SDRAM
- Block write and masked write instructions.

DDR1

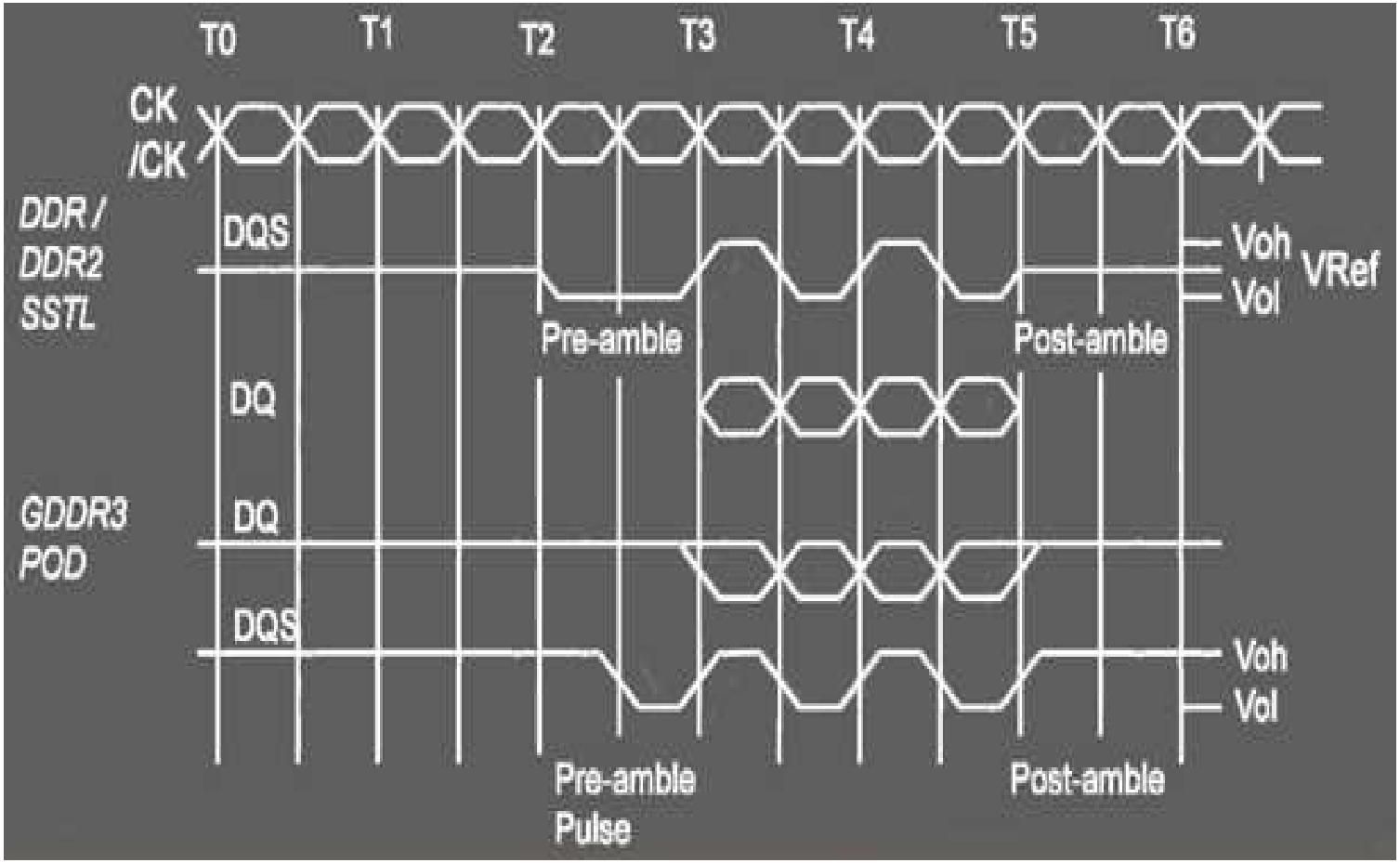
- Many boards used just plain DDR1

GDDR2

- Actually finalized before DDR2 was
- Point-to-point, allows increased speed.
- Needed to keep voltage same, with increased frequency caused higher power and thermal load.
- Abandoned pretty soon after introduction.

GDDR3

- Similar to GDDR2.
- Better than GDDR2 point to point. Complicated EE stuff. But in the end, the self-termination draws zero standby current wheras GDDR2 drew 11mA.
- On gddr3 strobe is always valid, don't have to wait for startup time.
- Unidirectional strobes (Read and write strobes separated)
- ODT (on chip termination) only for strobe signals,
- Only allows interleaved access mode, which simplifies controller? [instead of 0,1,2,3. . . you get 1,0 3,2 or 3,2 1,0. Apparently sequential mode is legacy but current DRAM's support both.


T0
T1
T2
T3
T4
T5
T6
CK
/CK
DDR /
DDR2
SSTL
DQS
Voh
Vol
VRef
Pre-amble
Post-amble
DQ
GDDR3
POD
DQ
DQS
Voh
Vol
Pre-amble
Pulse
Post-amble

Comparison Table

Feature	DDR	GDDR2	GDDR3
I/O	SSTL-2	SSTL-18 w ODT	POD-18
Clocking Interface	DQS	DQS or Diff DQS	Unidirectional DQS
Data Rate	200-600Mhz	400-667Mhz	more than 600MHz

SSTL-2/18 (2=2.5V, 18=1.8V)
SSTL = Stub Series Terminator Logic
POD = (Pseudo-Open Drain). At idle strobes are high, so no current drain?
ODT = On Die Termination