

ECE 571 – Advanced Microprocessor-Based Design Lecture 37

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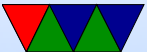
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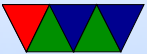
Announcements

- Will update you on project status
- Reminder: no final



PCIe

- But first some history



Some Old Desktop Busses

- Directly connected to CPU addr/data bus
- S100 – 100 pins (Altair, z80, 8080)
- Apple II – 50 pins (6502)
- ISA – 68 pins (8086)
 - 4.7MHz – problem when faster
 - 8-bit, extended to 16-bit



Move to 32-bit

- 486 timeframe
- IBM PS/2, with Microchannel (MCA) bus. Proprietary. Didn't take off
- EISA slot – extra pins stuck down inside regular ISA connector
- VLB – Vesa Local bust, for video cards. Extra (MCA-shaped) connector



PCI

- Peripheral Component Interconnect
- 32-bit parallel, 33MHz, 5V, 133MB/s
- Shared bus, take turns
- PCI 1.0 – 64 bit option (never popular)
- PCI 2.0 – 3.3v (keyed notch flipped, could have cards do both)
- PCI 2.1 – 66MHz
- PCI-X 133MHz
- AGP – mostly compatible with PCI for graphics card.



- No sharing, faster speed
- Accelerated DMA-like access to memory (GART)



Why is Parallel Bad at Fast Speeds?



PCIe

- PCI express – 2004
- High-speed serial replacement
- Point-to-point (not shared)
- Packets (like network)
- Vaguely backwards compatible at software level with PCI
- One to 32 lanes. Data striped across lanes.
- PCI-X (133MHz, 64-bit) and PCIe 1.0 x4 roughly same speed 1064 MB/s, PCIe win if many cards going or full duplex



- Each lane has 4-wires (differential pair in each direction)



PCIe versions

Ver	Year	Prot	Speed	x1	x16
1.0	2003	8b/10b	2.5GT/s	~0.25 GB/s	~4 GB/s
2.0	2007	8b/10b	5.0GT/s	~0.5 GB/s	~8 GB/s
3.0	2010	128b/130b	8.0T/s	~1.0 GB/s	~16 GB/s
4.0	2017	128b/130b	16.0GT/s	~2.0 GB/s	~32 GB/s
5.0	2019	128b/130b	32.0GT/s	~4.0 GB/s	~64 GB/s
6.0	2021	PAM4/ECC	64GT/s	~8.0 GB/s	~128 GB/s



Power

- All 3A at 3.3W (10W)
 - x1 = 0.5W at 12V = 6W
(full-sized can negotiate more?)
 - x4 = 2.1W at 12V = 25W
 - x16 = 5.5W at 12V = 66W (+10W = 75W)
- 8-pin connector for power supply direct connect (why at 12v?) to provide up to 375W

