**The following is copied from "STM32L15xxx reference manual (RM0038)."**

## LCD Register Map

| Offset | Register | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x00 | **LCD_CR** | Reserved | | | | | | | | | | | | | | | | | | | | | | | | MUX_SEG | BIAS[1:0] | | DUTY[2:0] | | | VSEL | LCDEN |
| | Reset value | | | | | | | | | | | | | | | | | | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x04 | **LCD_FCR** | Reserved | | | | | | PS[3:0] | | | | DIV[3:0] | | | | BLINK[1:0] | | BLINKF[2:0] | | | | CC[2:0] | | | DEAD [2:0] | | PON[2:0] | | | UDDIE | Reserved | SOFIE | HD |
| | Reset value | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 |
| 0x08 | **LCD_SR** | Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | FCRSF | RDY | UDD | UDR | SOF | ENS |
| | Reset value | | | | | | | | | | | | | | | | | | | | | | | | | | | 1 | 0 | 0 | 0 | 0 | 0 |
| 0x0C | **LCD_CLR** | Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | | UDDC | Reserved | SOFC | Reserved |
| | Reset value | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 0 | | 0 | |
| 0x14 | **LCD_RAM (COM0)** | S31 | S30 | S29 | S28 | S27 | S26 | S25 | S24 | S23 | S22 | S21 | S20 | S19 | S18 | S17 | S16 | S15 | S14 | S13 | S12 | S11 | S10 | S09 | S08 | S07 | S06 | S05 | S04 | S03 | S02 | S01 | S00 |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x18 | | Reserved | | | | | | | | | | | | | | | | | | | | S43 | S42 | S41 | S40 | S39 | S38 | S37 | S36 | S35 | S34 | S33 | S32 |
| | | | | | | | | | | | | | | | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x1C | **LCD_RAM (COM1)** | S31 | S30 | S29 | S28 | S27 | S26 | S25 | S24 | S23 | S22 | S21 | S20 | S19 | S18 | S17 | S16 | S15 | S14 | S13 | S12 | S11 | S10 | S09 | S08 | S07 | S06 | S05 | S04 | S03 | S02 | S01 | S00 |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x20 | | Reserved | | | | | | | | | | | | | | | | | | | | S43 | S42 | S41 | S40 | S39 | S38 | S37 | S36 | S35 | S34 | S33 | S32 |
| | | | | | | | | | | | | | | | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x24 | **LCD_RAM (COM2)** | S31 | S30 | S29 | S28 | S27 | S26 | S25 | S24 | S23 | S22 | S21 | S20 | S19 | S18 | S17 | S16 | S15 | S14 | S13 | S12 | S11 | S10 | S09 | S08 | S07 | S06 | S05 | S04 | S03 | S02 | S01 | S00 |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x28 | | Reserved | | | | | | | | | | | | | | | | | | | | S43 | S42 | S41 | S40 | S39 | S38 | S37 | S36 | S35 | S34 | S33 | S32 |
| | | | | | | | | | | | | | | | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x2C | **LCD_RAM (COM3)** | S31 | S30 | S29 | S28 | S27 | S26 | S25 | S24 | S23 | S22 | S21 | S20 | S19 | S18 | S17 | S16 | S15 | S14 | S13 | S12 | S11 | S10 | S09 | S08 | S07 | S06 | S05 | S04 | S03 | S02 | S01 | S00 |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x30 | | Reserved | | | | | | | | | | | | | | | | | | | | S43 | S42 | S41 | S40 | S39 | S38 | S37 | S36 | S35 | S34 | S33 | S32 |
| | | | | | | | | | | | | | | | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x34 | **LCD_RAM (COM4)** | S31 | S30 | S29 | S28 | S27 | S26 | S25 | S24 | S23 | S22 | S21 | S20 | S19 | S18 | S17 | S16 | S15 | S14 | S13 | S12 | S11 | S10 | S09 | S08 | S07 | S06 | S05 | S04 | S03 | S02 | S01 | S00 |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x38 | | Reserved | | | | | | | | | | | | | | | | | | | | | | | | S39 | S38 | S37 | S36 | S35 | S34 | S33 | S32 |
| | | | | | | | | | | | | | | | | | | | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x3C | **LCD_RAM (COM5)** | S31 | S30 | S29 | S28 | S27 | S26 | S25 | S24 | S23 | S22 | S21 | S20 | S19 | S18 | S17 | S16 | S15 | S14 | S13 | S12 | S11 | S10 | S09 | S08 | S07 | S06 | S05 | S04 | S03 | S02 | S01 | S00 |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x40 | | Reserved | | | | | | | | | | | | | | | | | | | | | | | | S39 | S38 | S37 | S36 | S35 | S34 | S33 | S32 |
| | | | | | | | | | | | | | | | | | | | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x44 | **LCD_RAM** | S31 | S30 | S29 | S28 | S27 | S26 | S25 | S24 | S23 | S22 | S21 | S20 | S19 | S18 | S17 | S16 | S15 | S14 | S13 | S12 | S11 | S10 | S09 | S08 | S07 | S06 | S05 | S04 | S03 | S02 | S01 | S00 |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x48 | **(COM6)** | Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | S39 | S38 | S37 | S36 | S35 | S34 | S33 | S32 |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x4C | **LCD_RAM (COM7)** | S31 | S30 | S29 | S28 | S27 | S26 | S25 | S24 | S23 | S22 | S21 | S20 | S19 | S18 | S17 | S16 | S15 | S14 | S13 | S12 | S11 | S10 | S09 | S08 | S07 | S06 | S05 | S04 | S03 | S02 | S01 | S00 |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x50 | | Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | S39 | S38 | S37 | S36 | S35 | S34 | S33 | S32 |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## 15.5.1 LCD control register (LCD_CR)

Address offset: 0x00

Reset value: 0x0000 0000

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | | | | MUX_SEG | BIAS[1:0] | | DUTY[2:0] | | | VSEL | LCDEN | |
| | | | | | | | rw/r | rw/r | rw/r | rw/r | rw/r | rw/r | rw/r | rw | |

Bits 31:8 Reserved, must be kept at reset value

Bit 7 **MUX_SEG**: Mux segment enable

This bit is used to enable SEG pin remapping. Four SEG pins can be multiplexed with SEG[31:28]. See *Section 15.4.7*.

0: SEG pin multiplexing disabled
1: SEG[31:28] are multiplexed with SEG[43:40]

Bits 6:5 **BIAS[1:0]**: Bias selector

These bits determine the bias used. Value 11 is forbidden.

00: Bias 1/4
01: Bias 1/2
10: Bias 1/3
11: Reserved

Bits 4:2 **DUTY[2:0]**: Duty selection

These bits determine the duty cycle. Values 101, 110 and 111 are forbidden.

000: Static duty
001: 1/2 duty
010: 1/3 duty
011: 1/4 duty
100: 1/8 duty
101: Reserved
110: Reserved
111: Reserved

Bit 1 **VSEL**: Voltage source selection

The VSEL bit determines the voltage source for the LCD.

0: Internal source (voltage step-up converter)
1: External source ($V_{LCD}$ pin) Bit 0

**LCDEN**: LCD controller enable

This bit is set by software to enable the LCD Controller/Driver. It is cleared by software to turn off the LCD at the beginning of the next frame. When the LCD is disabled all COM and SEG pins are driven to $V_{SS}$.

0: LCD Controller disabled

1: LCD Controller enabled

*Note: The VSEL, MUX_SEG, BIAS and DUTY bits are write protected when the LCD is enabled (ENS bit in LCD_SR to 1).*

## 15.5.2 LCD frame control register (LCD_FCR)

Address offset: 0x04

Reset value: 0x0000 0000

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reserved | | | | | PS[3:0] | | | | DIV[3:0] | | | | BLINK[1:0] | | |
| | | | | | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BLINKF[2:0] | | | CC[2:0] | | | DEAD[2:0] | | | PON[2:0] | | | UDDIE | Res. | SOFIE | HD |
| rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | | rw | rw |

Bits 31:26 Reserved, must be kept at reset value

Bits 25:22 **PS[3:0]**: PS 16-bit prescaler

These bits are written by software to define the division factor of the PS 16-bit prescaler. ck_ps = LCDCLK/(2). See *Section 15.4.2*.

0000: ck_ps = LCDCLK

0001: ck_ps = LCDCLK/2

0002: ck_ps = LCDCLK/4

...

1111: ck_ps = LCDCLK/32768

Bits 21:18 **DIV[3:0]**: DIV clock divider

These bits are written by software to define the division factor of the DIV divider. See *Section 15.4.2*.

0000: ck_div = ck_ps/16

0001: ck_div = ck_ps/17

0002: ck_div = ck_ps/18

...

1111: ck_div = ck_ps/31

Bits 17:16 **BLINK[1:0]**: Blink mode selection

00: Blink disabled

01: Blink enabled on SEG[0], COM[0] (1 pixel)

10: Blink enabled on SEG[0], all COMs (up to 8 pixels depending on the programmed duty)

11: Blink enabled on all SEGs and all COMs (all pixels)

Bits 15:13 **BLINKF[2:0]**: Blink frequency selection

000: $f_{LCD}$/8

001: $f_{LCD}$/16

010: $f_{LCD}$/32

011: $f_{LCD}$/64

100: $f_{LCD}$/128

101: $f_{LCD}$/256

110: $f_{LCD}$/512

111: $f_{LCD}$/1024

Bits 12:10 **CC[2:0]**: Contrast control

These bits specify one of the $V_{LCD}$ maximum voltages (independent of $V_{DD}$). It ranges from 2.60 V to 3.51V.
000: $V_{LCD0}$100: $V_{LCD4}$
001: $V_{LCD1}$101: $V_{LCD5}$
010: $V_{LCD2}$110 $V_{LCD6}$
011: $V_{LCD3}$111: $V_{LCD7}$

*Note: Refer to the product datasheet for the $V_{LCDx}$ values.*

Bits 9:7 **DEAD[2:0]**: Dead time duration

These bits are written by software to configure the length of the dead time between frames. During the dead time the COM and SEG voltage levels are held at 0 V to reduce the contrast without modifying the frame rate.
000: No dead time
001: 1 phase period dead time
010: 2 phase period dead time
.....
111: 7 phase period dead time

Bits 6:4 **PON[2:0]**: Pulse ON duration

These bits are written by software to define the pulse duration in terms of ck_ps pulses. A short pulse will lead to lower power consumption, but displays with
high internal resistance may need a longer pulse to achieve satisfactory contrast. Note that the pulse will never be longer than one half prescaled LCD clock period.

| | |
|---|---|
| 000: 0 | 100: 4/ck_ps |
| 001: 1/ck_ps | 101: 5/ck_ps |
| 010: 2/ck_ps | 110: 6/ck_ps |
| 011: 3/ck_ps | 111: 7/ck_ps |

PON duration example with LCDCLK = 32.768 kHz and PS=0x03:

| | |
|---|---|
| 000: 0 µs | 100: 976 µs |
| 001: 244 µs | 101: 1.22 ms |
| 010: 488 µs | 110: 1.46 ms |
| 011: 782 µs | 111: 1.71 ms |

Bit 3 **UDDIE**: Update display done interrupt enable

This bit is set and cleared by software.
0: LCD Update Display Done interrupt disabled
1: LCD Update Display Done interrupt enabled

Bit 2 Reserved, must be kept at reset value

Bit 1 **SOFIE**: Start of frame interrupt enable

This bit is set and cleared by software.
0: LCD Start of Frame interrupt disabled
1: LCD Start of Frame interrupt enabled

Bit 0 **HD**: High drive enable

This bit is written by software to enable a low resistance divider. Displays with high internal resistance may need a longer drive time to achieve satisfactory contrast. This bit is useful in this case if some additional power consumption can be tolerated.
0: Permanent high drive disabled
1: Permanent high drive enabled. When HD=1, then the PON bits have to be programmed to 001.

*Note: The data in this register can be updated any time, however the new values are applied only at the beginning of the next frame (except for CC, UDDIE, SOFIE that affect the device behavior immediately).*

*Reading this register obtains the last value written in the register and not the configuration used to display the current frame.*

### 15.5.3 LCD status register (LCD_SR)

Address offset: 0x08

Reset value: 0x0000 0020

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | | | | | | FCRSF | RDY | UDD | UDR | SOF | ENS | |
| | | | | | | | | | r | r | r | rs | r | r | |

Bits 31:6 Reserved, must be kept at reset value

Bit 5 **FCRSF**: LCD Frame Control Register Synchronization flag

This bit is set by hardware each time the LCD_FCR register is updated in the LCDCLK domain. It is cleared by hardware when writing to the LCD_FCR register.

0: LCD Frame Control Register not yet synchronized

1: LCD Frame Control Register synchronized

Bit 4 **RDY**: Ready flag

This bit is set and cleared by hardware. It indicates the status of the step-up converter.

0: Not ready

1: Step-up converter is enabled and ready to provide the correct voltage.

Bit 3 **UDD**: Update Display Done

This bit is set by hardware. It is cleared by writing 1 to the UDDC bit in the LCD_CLR register. The bit set has priority over the clear.

0: No event

1: Update Display Request done. A UDD interrupt is generated if the UDDIE bit in the LCD_FCR register is set.

*Note: If the device is in STOP mode (PCLK not provided) UDD will not generate an interrupt even if UDDIE = 1.*

*If the display is not enabled the UDD interrupt will never occur.*

Bit 2 **UDR**: Update display request

Each time software modifies the LCD_RAM it must set the UDR bit to transfer the updated data to the second level buffer. The UDR bit stays set until the end of the update and during this time the LCD_RAM is write protected.

0: No effect

1: Update Display request

*Note: When the display is disabled, the update is performed for all LCD_DISPLAY locations. When the display is enabled, the update is performed only for locations for which commons are active (depending on DUTY). For example if DUTY = 1/2, only the LCD_DISPLAY of COM0 and COM1 will be updated.*

*Note: Writing 0 on this bit or writing 1 when it is already 1 has no effect. This bit can be cleared by hardware only. It can be cleared only when LCDEN = 1*

Bit 1 **SOF**: Start of frame flag

This bit is set by hardware at the beginning of a new frame, at the same time as the display data is updated. It is cleared by writing a 1 to the SOFC bit in the LCD_CLR register. The bit clear has priority over the set.

0: No event

1: Start of Frame event occurred. An LCD Start of Frame Interrupt is generated if the SOFIE bit is set.

Bit 0 **ENS**: LCD enabled status

This bit is set and cleared by hardware. It indicates the LCD controller status.

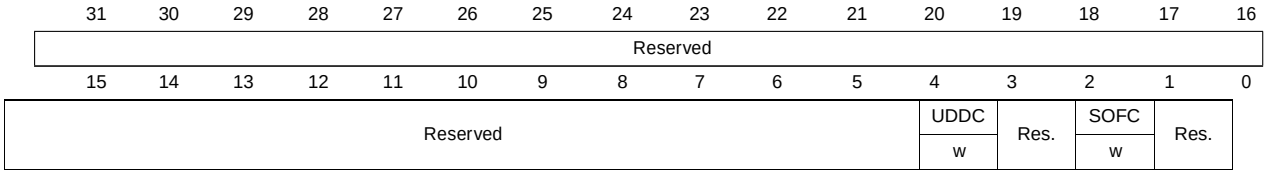
0: LCD Controller disabled.
1: LCD Controller enabled

*Note: The ENS bit is set immediately when the LCDEN bit in the LCD_CR goes from 0 to 1. On deactivation it reflects the real status of LCD so it becomes 0 at the end of the last displayed frame.*

### 15.5.4 LCD clear register (LCD_CLR)

Address offset: 0x0C Reset value:

0x0000 0000




Bit 31:2 Reserved, must be kept at reset value

Bit 3 **UDDC:** Update display done clear
This bit is written by software to clear the UDD flag in the LCD_SR register.
0: No effect
1: Clear UDD flag

Bit 2 Reserved, must be kept at reset value

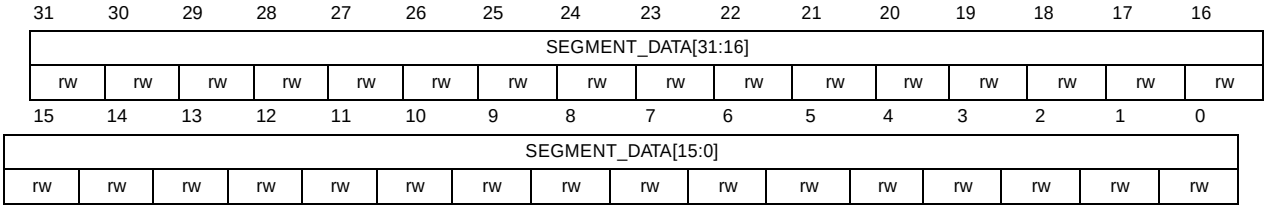
Bit 1 **SOFC:** Start of frame flag clear
This bit is written by software to clear the SOF flag in the LCD_SR register.
0: No effect
1: Clear SOF flag

Bit 0 Reserved, must be kept at reset value

### 15.5.5 LCD display memory (LCD_RAM)

Address offset: 0x14-0x50

Reset value: 0x0000 0000




Bits 31:0 **SEGMENT_DATA[31:0]**
Each bit corresponds to one pixel of the LCD display.
0: Pixel inactive
1: Pixel active