Multi-Band Digital to Analog Converter Compensation

By
Ryan C. Jacobson

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Advisory Committee:

Donald M. Hummels, Associate Professor of Electrical and Computer Engineering, Advisor

Fred H. Irons, Castle Professor of Electrical and Computer Engineering

Allison I. Whitney, Lecturer in Electrical and Computer Engineering

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Thesis Advisor: Dr. Donald M. Hummels

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Digital-to-Analog Converters (DACs) have become a necessary building block for modern communication systems. DACs are needed in many systems including broadband computer modems, mobile cellular phone networks, complex waveform generators, and feedback loops of high performance Analog-to-Digital Converters (ADCs); all systems which require high-performance. These systems are moving to higher and higher speeds while still requiring the same output accuracy. Unfortunately, DACs have several limitations which make meeting the stringent demands difficult.

The DAC's translation of a digital sequence to an analog waveform is not ideal, introducing harmonic error in the output. This thesis develops hardware and a multi-band procedure to reduce the harmonic error in the DAC output. The multi-band procedure incorporates two frequency bands of the DAC output spectrum to create an error characteristic. This error characteristic can be used to correct the input samples of the DAC to reduce the harmonic distortion in the output. Hardware is developed to implement the procedure in commercially available DACs. Rewarding results were found in both simulated and hardware tests.

ACKNOWLEDGMENTS

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

CHAPTER 1

Introduction

Digital-to-Analog Converters (DACs) have become a necessary building block for modern communication systems. DACs are needed in many systems including broadband computer modems, mobile cellular phone networks, complex waveform generators, and feedback loops of high performance Analog-to-Digital Converters (ADCs); all systems which require high-performance. These systems are moving to higher and higher speeds while still requiring the same output accuracy. Unfortunately, DACs have many limitations which make meeting the stringent demands difficult. This need for high speed, high-performance DACs motivates the development of methods to improve a DAC's operation.

1.1 Background

DAC calibration poses a fundamental problem of obtaining a measure of the errors present across the DAC output spectrum. Ideally one would use an ADC to sample the DAC output, both having the same clock rate, allowing a full band measurement of the error. Unfortunately, to obtain enough resolution to measure the errors in the DAC output, the ADC must be clocked at a much slower speed as ADCs have inadequate resolution at the required DAC clock frequency. This only allows for error measurements in a small portion of the entire DAC output spectrum.

One previous attempt which provided some useful results has investigated this problem [6] . The approach made use of lowpass measurements to create an error characteristic (assumed to be a function of the current input code and previous input code) for the DAC. The error characteristic was then used to modify the input samples to the DAC in attempt to reduce harmonic distortion in the output spectrum. A hardware implementation of the calibration system was built to test the approach. Unfortunately the quality of the hardware setup was less than ideal making it difficult to produce repeatable results. However, the quality of the setup was good enough to see the effects of the lowpass measurement approach. Indeed, some harmonic distortion was removed from the output but much distortion was left untouched. These shortcomings are the motivation for the development of this thesis. Not only did the repeatability of experiments need to be improved, but a method of creating a better error characteristic which characterized the full band of the DAC had to be created.

1.2 Purpose of This Research

This thesis is basically a continuation of Kirk Riley's work [6] done at the Communications Lab at the University of Maine. The overall goal of the project is to improve the performance of components required to implement an all digital receiver, part of the Digital Receiver Technology Program funded by the Defense Advanced Research Projects Agency (DARPA).

> "The goal of the Digital Receiver Technology Program is to demonstrate receivers with enhanced performance, programmability, reliability and maintainability, and reduced size, weight, power, and cost. The accomplishment of this goal will lead to entirely new defense system capabilities such as unmanned air vehicles (UAVs) with sophisticated electronic payloads." [4]

The DAC is an integral part of a digital receiver. Not only is the DAC used in the conversion of digital words into analog voltages to create complex waveforms in the receiver, it is also used in the feedback loops of modern high-performance ADC architectures.

The use of the DAC is further emphasized in the design of an adaptive, self calibrating receiver where well defined calibration signals are required.

Because the digital receiver is expected to require high speed, high resolution DACs the Communications Lab was called upon to investigate compensating DACs. This thesis serves as a stepping stone in understanding and correcting errors inherent in modern DAC designs.

1.3 Thesis Organization

This thesis develops a method to modify a DAC's input sequence producing an output with distortion reduced throughout the entire Nyquist band of the DAC. By using an ADC with a lower clock rate, an accurate measure of the DAC errors can be made. Processes to measure and correct the errors in the output are discussed.

Chapter 2 provides an overview of DAC calibration. A brief description and model of the errors present in the DAC output is introduced. Also presented is a summary and results of the previous attempt of DAC lowpass calibration in the Communications Lab. Finally the need for a second band of error information to perform a wideband DAC calibration is discussed.

Chapter 3 explains hardware considerations required for DAC calibration. In this chapter improvements over the previous hardware system can be seen. Also, Chapter 3 describes how the effects of the hardware are eliminated from the calibration scheme.

Chapter 4 presents the multi-band calibration technique used to obtain error information for several portions of the DAC output spectrum. Techniques used in calibration signal selection and calculation of the basis function weights are explained. The chapter concludes with an overview of the multi-band technique used to provide wideband DAC calibration is presented.

Chapter 5 provides results of both simulated and actual implementation of the calibration scheme.

Chapter 6 completes the thesis with some conclusions and possibilities for future work in this area.

CHAPTER 2

DAC Calibration Overview

This chapter provides a description of the current understanding of DAC errors and how these errors have been measured and calibrated. It continues on to show results from the current calibration scheme and the need for further improvement.

2.1 DAC Error

With few exceptions, most descriptions of distortion caused by DAC non-linearity involve static models of the DAC error [2]. That is, the error in the DAC output is assumed to be a function of the current DAC input only, and is assumed independent of the harmonic nature of the signal being created by the DAC. In practice, DACs produce distortion which depends on the dynamic properties of the input sequence, and dynamic error models must be used to accurately predict error versus frequency. This section introduces the error models used in this thesis.

2.1.1 Time Domain Dynamic Error Description

It is convenient to look at dynamic error in the time domain [2]. Figure 2.1 illustrates common dynamic specifications in the time domain by showing the deviation from an ideal step response. Shown in Figure 2.1 are four parameters; switching time, settling time, glitch impulse, and slew rate. Switching time is the amount of time needed for the DAC to obtain a certain level without settling. Settling time is the amount of time needed for the DAC output to stay within a certain percentage of the desired value. The glitch impulse is the measurement of the transient caused by the DAC's non-simultaneous action of current switches in the transition between input codes. The slew rate is the maximum rate of change

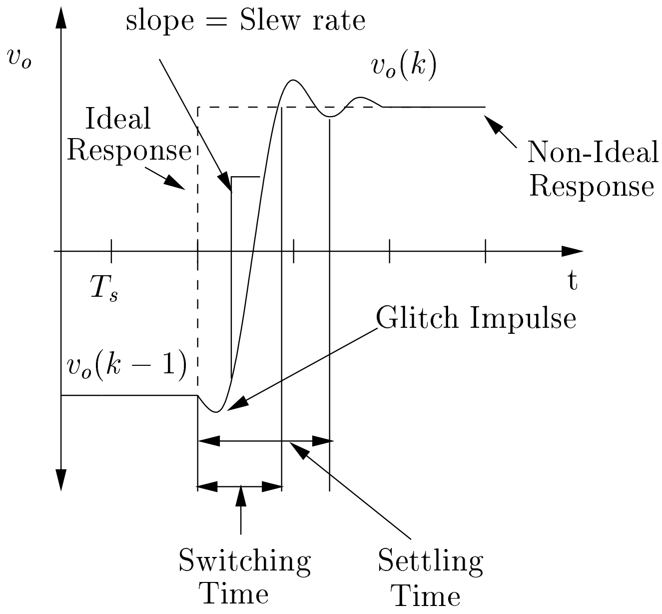

Figure 2.1: Time Domain Representation of Dynamic Errors

in the DAC's output stage. Even though these deviations from the ideal response will add distortion to the DAC's output, it is difficult to interpret and measure them in the time domain. Because of this it is necessary to look at the frequency domain to see if these errors manifest into harmonic distortion, which can then be measured.

2.1.2 Frequency Domain Dynamic Error Description

It is common for communication systems to be analyzed in the frequency domain. DAC nonlinearities may be easily identified by examining harmonic energy created by the DAC for input samples containing one or more sinusoids. One common measure of harmonic distortion is Spurious Free Dynamic Range (SFDR). This measure is best described graphically as illustrated in Figure 2.2. In this case, the DAC had been driven with a sinusoidal input sequence at 45.6 MHz. The output spectrum of the DAC has been measured and indicates several harmonic components (the largest of which is at 34.5 MHz). From Figure 2.2 it is

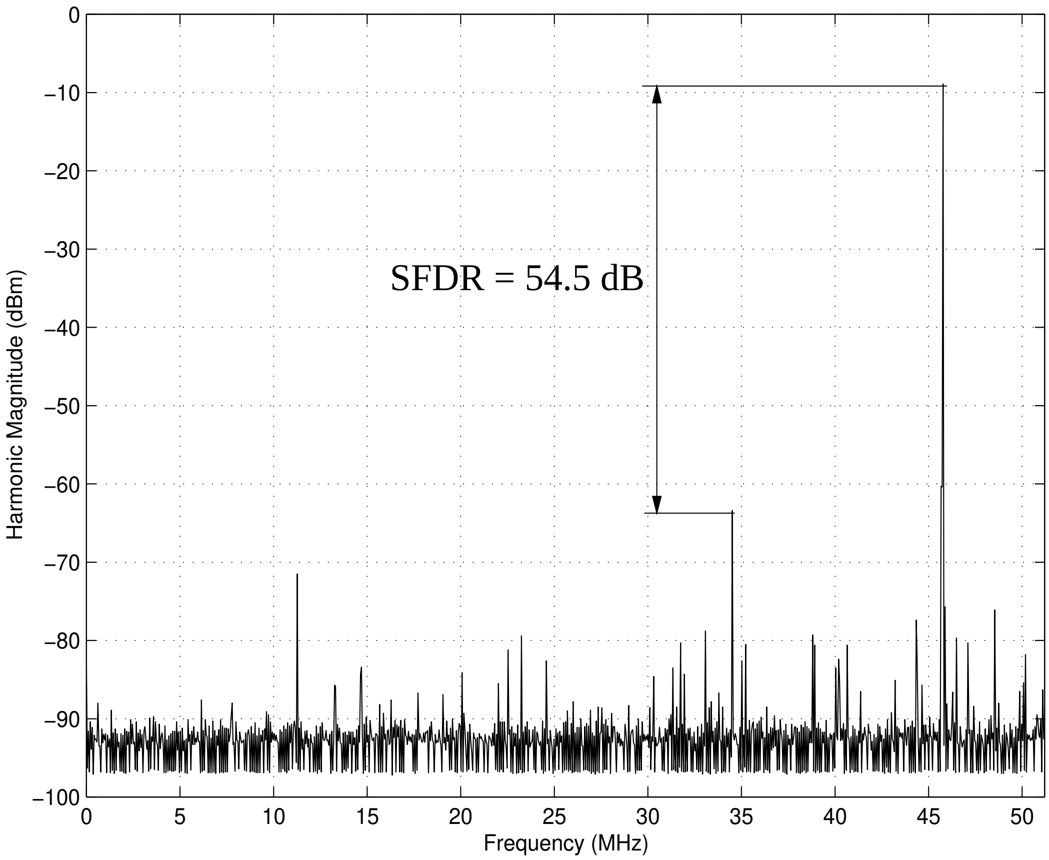

Figure 2.2: Graphical Interpretation of a SFDR Measurement

easy to see that SFDR is the difference of power levels (dB in this case) between the fundamental to the next highest distortion term. Ideally, one would like to have a large SFDR. Although it is actually very difficult to predict which dynamic errors are producing distortion terms, two important sources are output slewing limitations and bit transition errors.

Output slew limits can cause harmonic distortion at the output. The distortion is caused by the non-ideal change between states which is a function of the output stage of the DAC. As shown in Figure 2.1, the output ramps from one output voltage to the next. This ramping between output voltages causes harmonic distortion in the frequency domain as shown in Figure 2.3. Figure 2.3 shows a simulated DAC output spectrum for a slew-limited DAC. The simulated 102.4 MSPS DAC has 12 bits of resolution and an output slew rate of 12k ($12 * 1024$) Least Significant Bits (LSBs) per sample period, or 6 volts per sample period. It is important to note that this error is a function of the two most recent DAC input codes which will motivate an error model developed later in this thesis.

Bit transition errors are errors introduced in the output of the DAC due to internal mechanisms responsible for switching between output levels. Quite often bit transition errors, including glitches, are due to the current switches of the DAC output not changing simultaneously. A simulated DAC model can be developed to realize bit transition errors. This model is implemented by adding error which depends on whether certain DAC bits have changed state from one input code to the next. Such a model does produce error which can be observed in the frequency domain, shown in Figure 2.4. Again, it is important to note that these errors can be represented as a function of the the two most recent DAC inputs, again helping motivate the dynamic error model.

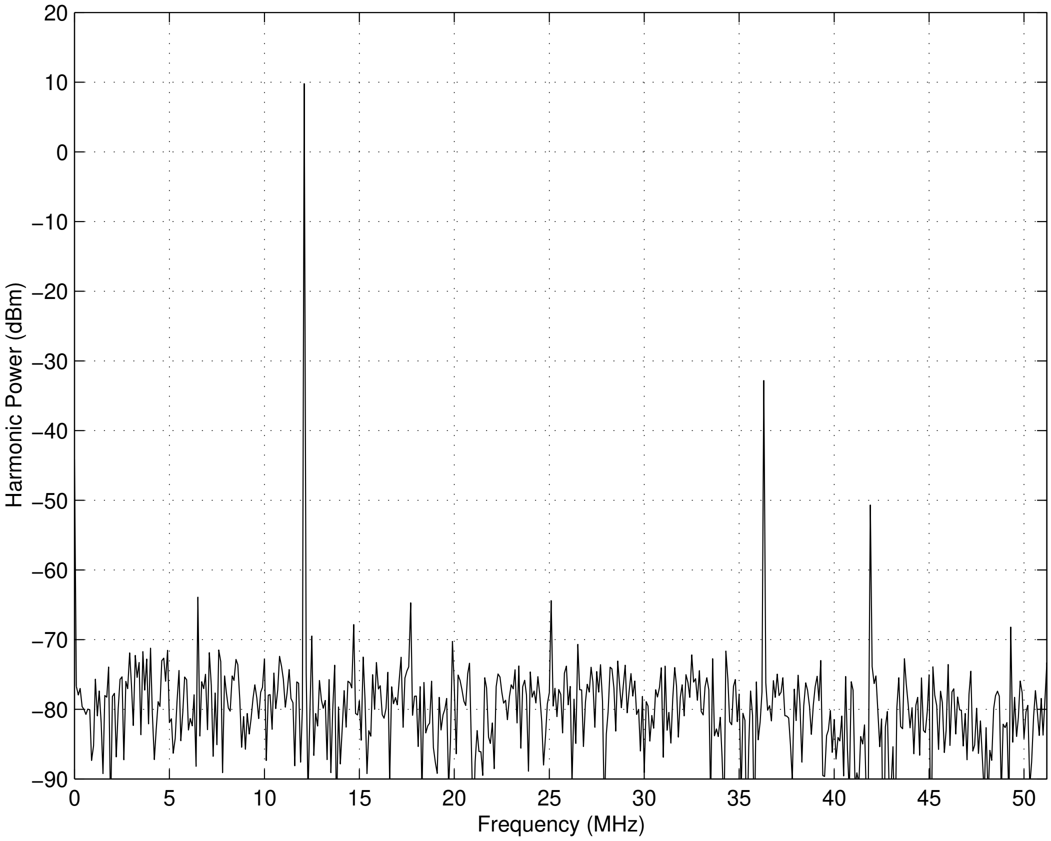

Figure 2.3: Output Spectrum Illustrating Slew Rate Error Distortion

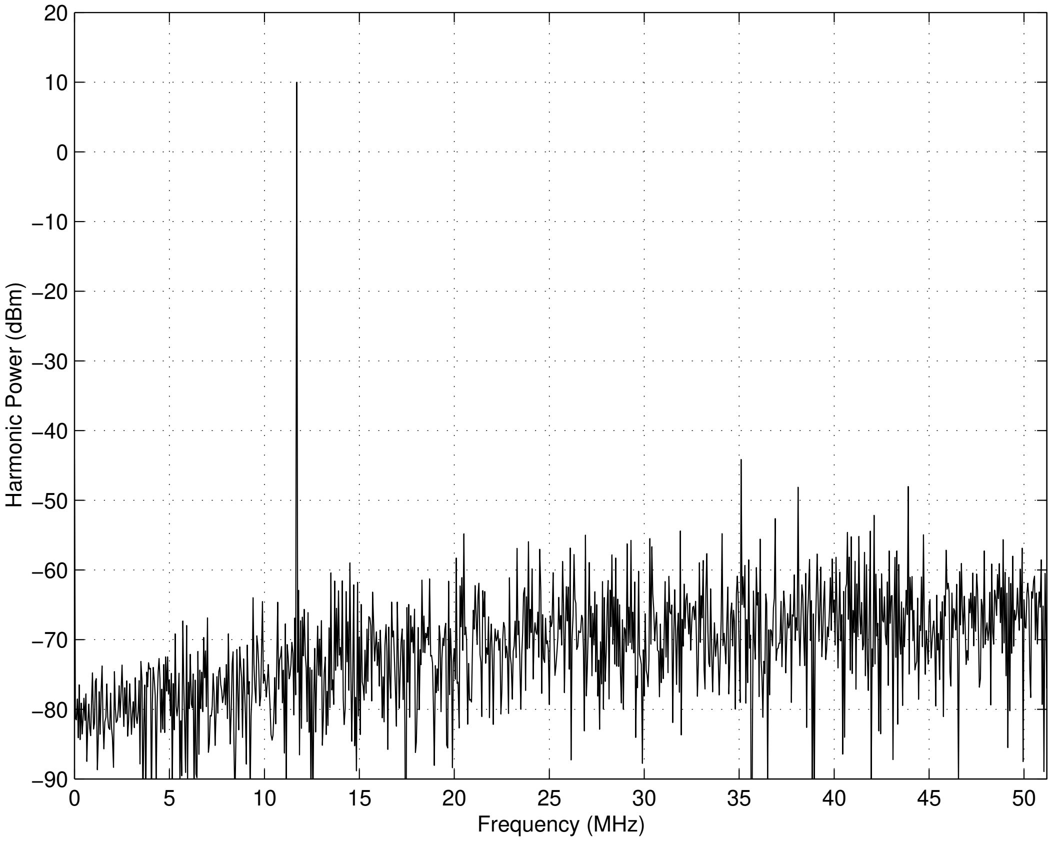

Figure 2.4: Output Spectrum Illustrating Bit Transition Error Distortion

2.1.3 DAC Error Model for Dynamic Distortion

Since the true effects of the dynamic distortion are difficult to foresee [2], it becomes necessary to develop a model for the dynamic error created by the non-ideal DAC. This can be accomplished through the use of an ideal DAC. An ideal DAC with a given input sequence

$$\ldots x_{k-1}, x_k, x_{k+1} \ldots \tag{2.1}$$

will have an output waveform, $v_o(t)$, after the reconstruction filter. For example, an input sequence which represents a unit step would produce a unit step in the output as shown by the ideal response in Figure 2.1.

In an ideal DAC, $v_o(t)$ is linearly related to the x_k sequence with $v_o(kT_s)$ (where T_s is the sampling period) being proportional to x_k. For a given input sequence, the non-ideal DAC output has the output of $v_o(t) + v_e(t)$, where $v_e(t)$ is introduced due to nonlinearities in the DAC. To model the non-ideal DAC output, a nonlinear modification of the input sequence to the ideal DAC can be made. This modification to the ideal DAC's input produces $v_o(t) + v_e(t)$ if the nonlinear modification, ϵ_k, is constructed correctly.

Since the dynamic error mechanisms in a DAC are dependent on transitions from the previous input codes to the current input code, a very general model for ϵ_k can be made.

$$\epsilon_k = e(x_k, x_{k-1}, x_{k-2}, x_{k-3}, \cdots). \tag{2.2}$$

However, it should be noted that, for most DACs, effects from $x_{k-2}, x_{k-3}, \cdots$ are small. This is due partly to the fact that DACs do not usually have much memory. The assumption that ϵ_k is only a function of the current input code and

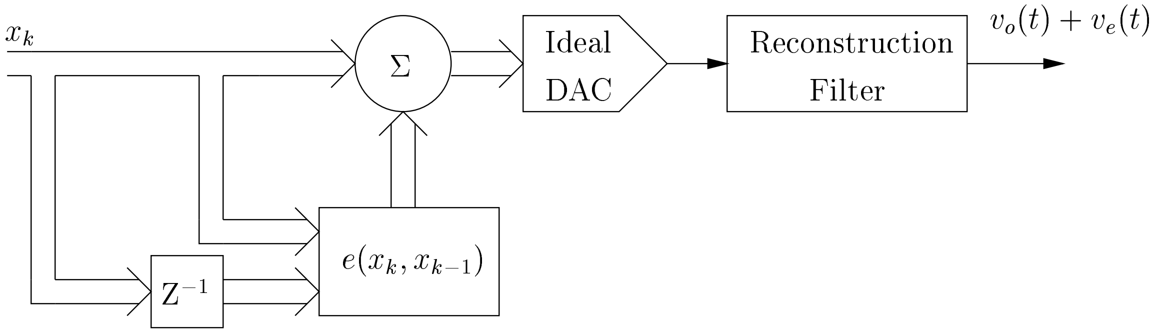

Figure 2.5: Dynamic DAC Model Diagram

the previous input code, or x_k and x_{k-1}, equation (2.3) is a simplification that captures the dominant errors.

$$\epsilon_k = e(x_k, x_{k-1}) \tag{2.3}$$

With ϵ_k defined, a dynamic DAC model can be constructed, shown in Figure 2.5. Using this model, both slew rate and bit transition errors can be modeled, as a function of state and previous state. With a valid model for dynamic distortion the next task at hand becomes the measurement and calibration of the error.

2.2 Lowpass Measurement and Calibration of DACs

Given a model for dynamic errors it becomes possible to correct a DAC's input sequence to give a desired (compensated) output. To calibrate the DAC's output, the nonlinear function $e(x_k, x_{k-1})$ must be determined. A previous scheme of DAC calibration [6] uses measurements from a lowpass system to estimate this nonlinearity.

One problem with DAC calibration is that the output is analog; a form that is of no use if one desires to use a computer for measuring the errors. To make the change to the digital world one must use an Analog-to-Digital Converter

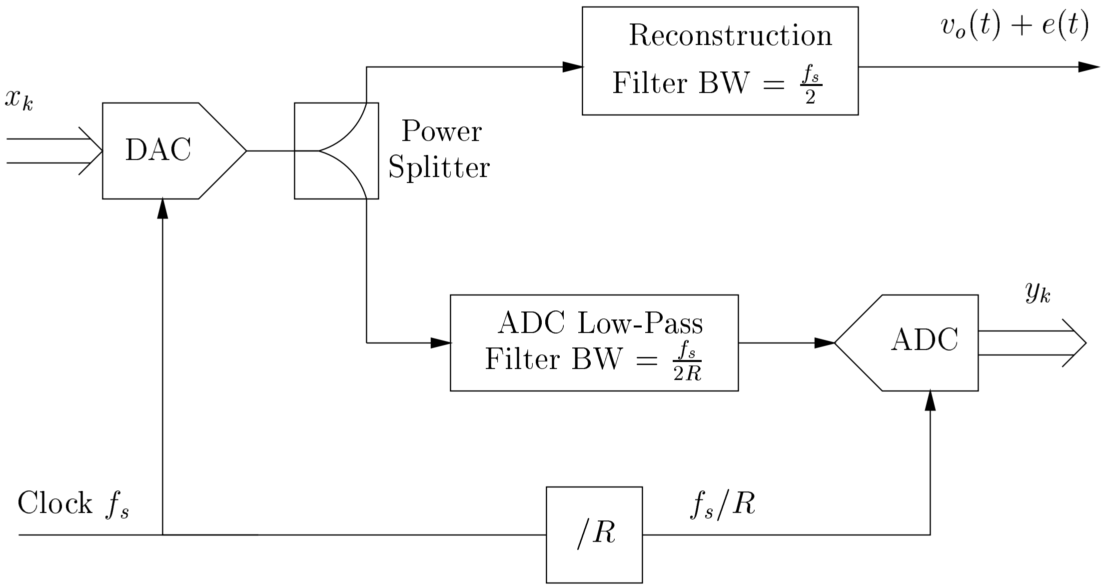

Figure 2.6: Lowpass Calibration System Diagram

(ADC) so that measurements made can be manipulated by computers. Ideally, it would be desirable to have an ADC which has higher resolution than the DAC. If this were the case, one could be certain that the error measured would be errors introduced by the DAC and not the ADC. However, an ADC of this type is not readily available for high-speed DACs. To achieve the required resolution it is necessary to sample the ADC at a lower clock rate than the DAC as shown in Figure 2.6.

In Figure 2.6 it can be seen that the ADC is being clocked by the DAC clock rate, f_s, divided by an integer R. The bandwidth of the ADC lowpass filter should also be noted. It is important to have a filter of bandwidth of at most $f_s/(2R)$ to filter all frequencies which would be outside of the Nyquist frequency ($0 < f < f_s/(2R)$) of the ADC. The filter's input impedance must also be matched to the output impedance of the DAC so that there will be a constant load for the DAC at all frequencies; reducing reflections for the filtered frequencies. Tests can be made to ensure that the ADC has adequate resolution at this clock frequency, f_s/R, with the lowpass filter in place. Also shown in Figure 2.6 is the hardware to observe the entire DAC's output spectrum by using a power splitter and reconstruction filter.

One limitation that this system presents is the Nyquist frequency limit of the ADC. Consider a DAC with f_s of 100 MHz. If R is equal to 4, then the sample rate of the ADC is 25 MHz. Whereas the DAC has a Nyquist frequency of 50 MHz, the ADC only has a Nyquist frequency of 12.5 MHz. Because of the Nyquist limitation of the ADC, the ADC filter must have a bandwidth of less than 12.5 MHz. This band, $0 \rightarrow 12.5$ MHz, becomes the only band of information available to use to calibrate the DAC. The goal is that it will be possible to estimate the DAC error characteristic from this small measurement band.

With the system of Figure 2.6 it is possible to measure the DAC frequency distortion terms that fall into the band of the lowpass reconstruction filter. By knowing the input sequence to the DAC, one can compare the ideal input spectrum to that of the corrupted output spectrum. To relate the spectra, a Discrete Fourier Transform (DFT) [5] must be calculated for both the input and output sequences. For a sequence of length N

$$x_o, x_1, x_2, \ldots x_{N-1}, \tag{2.4}$$

the DFT is defined by

$$X_n = \sum_{i=0}^{N-1} x_i e^{-j2\pi ni/N} \qquad n = 0, 1, \ldots N-1. \tag{2.5}$$

A matrix notation for the DFT may be constructed by defining a matrix $\tilde{T}$ such that $\tilde{T}\vec{x}$ returns the Fourier Transform of $\vec{x}$, or $\vec{X}$ where

$$\vec{x} = \begin{bmatrix} x_0 & x_1 & \ldots & x_{N-1} \end{bmatrix}^T \tag{2.6}$$

and

$$\vec{X} = \begin{bmatrix} X_0 & X_1 & \dots & X_{N-1} \end{bmatrix}^T. \tag{2.7}$$

The elements of $\tilde{T}$ are created by

$$\tilde{T} = \begin{bmatrix} {W_N}^0 & {W_N}^0 & {W_N}^0 & \dots & {W_N}^0 \\ {W_N}^0 & {W_N}^{1*1} & {W_N}^{1*2} & \dots & {W_N}^{1*(N-1)} \\ {W_N}^0 & {W_N}^{2*1} & {W_N}^{2*2} & \dots & {W_N}^{2*(N-1)} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ {W_N}^0 & {W_N}^{(N-1)*1} & {W_N}^{(N-1)*2} & \dots & {W_N}^{(N-1)*(N-1)} \end{bmatrix} \tag{2.8}$$

where

$$W_N = e^{-j\frac{2\pi}{N}}. \tag{2.9}$$

Construction of $\tilde{T}$ allows $\vec{X}$ to be symbolically derived from $\vec{x}$. It is this transform to the frequency domain that allows the calibration routine to identify errors in the frequency domain.

By comparing the input and output spectra the dynamic errors of the DAC within the bandwidth of the reconstruction filter will be revealed. With this information obtained, a DAC error characteristic, based on current input code and previous input code transitions, can be obtained which then can be used to adjust the DAC input sequence.

Assuming that a model for the error associated with all combinations of current input - previous input has been calculated, the input sequence, $\vec{x}$, to the DAC can be modified ($\vec{x}_c$) to obtain the desired output. To do this, $\vec{y}_d$, the desired output which has no harmonics, must be compared with $\vec{y}_e$, the estimated output derived from the error model. $\vec{y}_d$ can be calculated from the input values, $\vec{x}$, shown in equation (2.10).

$$\vec{y}_d = C + P\vec{x} \tag{2.10}$$

Here, C is a constant offset term and P is a proportionality constant which appropriates the correct amount of voltage per DAC LSB. Likewise, $\vec{y}_e$ can be calculated from the calibrated input samples, $\vec{x}_c$ and the associated error characteristic, $e(\vec{x}_c, \vec{x}_c^{(-1)})$ where $\vec{x}_c^{(-1)}$ is the set of previous, calibrated input samples.

$$\vec{y}_e = C + P(\vec{x}_c + e(\vec{x}_c, \vec{x}_c^{(-1)})) \tag{2.11}$$

The correct $\vec{x}_c$ is the input vector which minimizes the error between $\vec{y}_d$ and $\vec{y}_e$. This can be done with an iterative search for the best input vector, $\vec{x}_c$. This is the previous approach of DAC calibration and the next section explains where this approach fails and the need for information in another band of frequencies.

2.3 Failure of Lowpass Calibration

The lowpass calibration scheme described in Section 2.2 has provided successful results . Unfortunately, the lowpass information does not seem to be enough to calibrate the full band of the DAC [6]. This leads to the need of measurement of other bands of information to extend the DAC error characteristic to include the full band of the DAC's output.

2.3.1 Results from Lowpass Calibration

The following results were produced from the lowpass calibration described in Section 2.2 which represents the most current work the Communications Lab had completed in DAC calibration [6]. A system was constructed that followed the framework shown in Figure 2.6. The DAC being tested is the Tektronics TDKA30P 12-bit DAC sampled at a frequency of 100 MHz. The input samples which represented a five-tone test pattern were provided by a Hewlett Packard HP16522A pattern generator. The divide factor R was chosen to be 4. This gave the ADC, an Analog Devices AD9042D 12-bit ADC, a sampling frequency of 25 MHz. The bandwidth of an elliptic lowpass filter was chosen to be 6.3 MHz and a matching network was constructed to provide a more constant load impedance for the DAC. The data produced by the ADC was captured by the Tektronics 9504 data cache. The output spectrum of the DAC is captured by the Hewlett Packard HP 8568B Spectrum Analyzer. Figure 2.7 shows the uncompensated DAC output for the system. Note that the DAC noise floor shown in Figure 2.7 is at about -84 dBm. Secondly, a tone at 25 MHz is present. This tone is due to the clock generated for the ADC. Both of these signal degradations are due to circuit implementation details which and are addressed in this thesis.

Figure 2.8 shows a compensated DAC output spectrum for the above experiment. Note that the observation band of 6.3 MHz was nearly compensated. Unfortunately the entire band was not compensated. It is encouraging that the observation band was compensated as the information in that band was used as a model for the DAC error characteristic. The DAC error characteristic developed only includes dynamic DAC errors that produce energies at low frequencies. These results show the need for another band of information to better produce a DAC error characteristic which will compensate the entire band of the DAC's output.

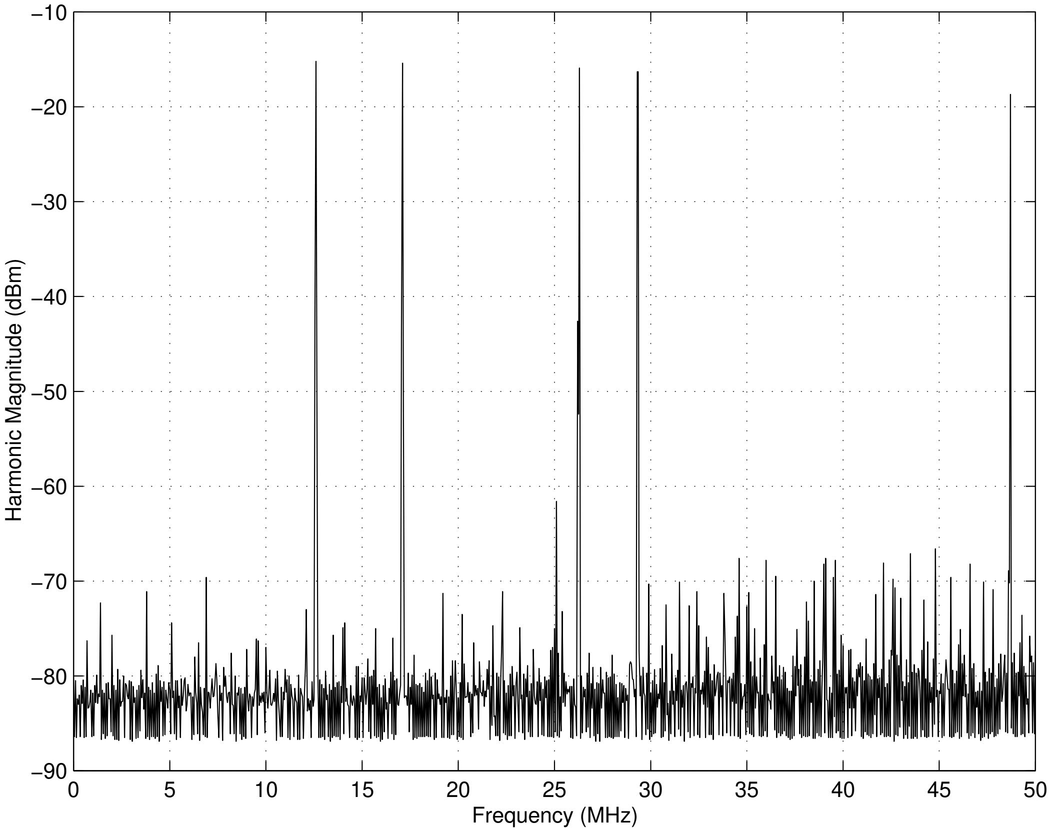

Figure 2.7: Original Hardware Uncompensated DAC Output Spectrum.

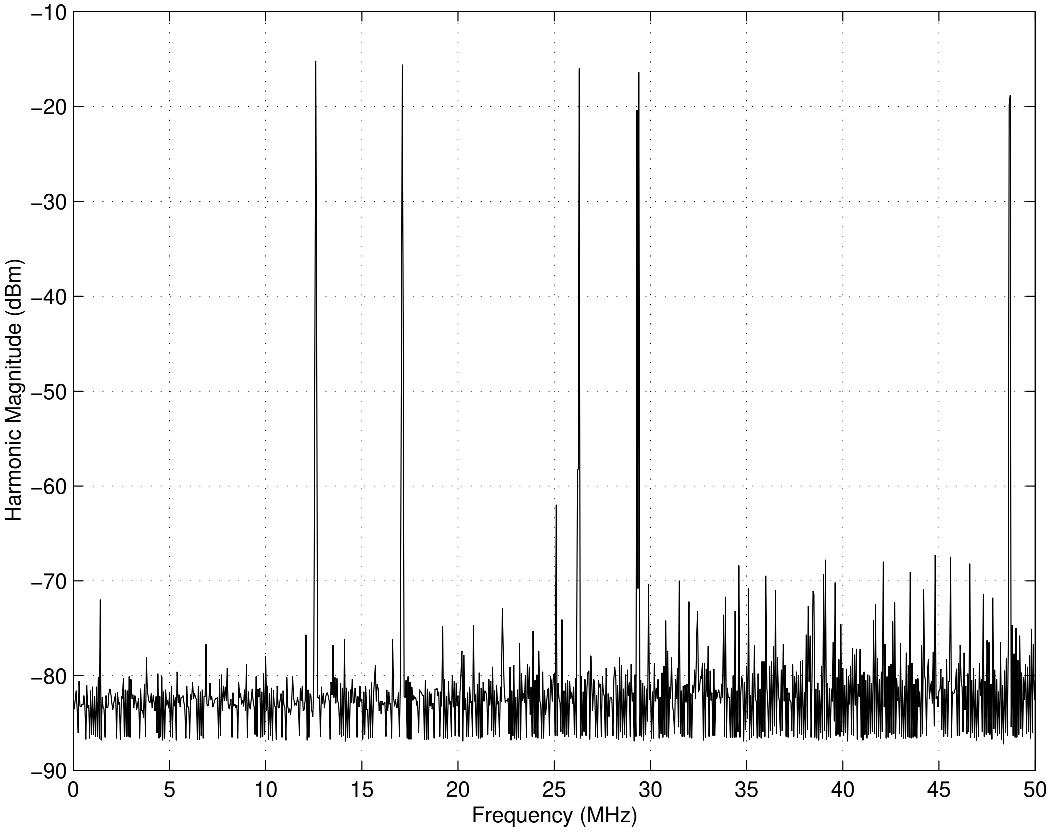

Figure 2.8: Original Hardware Compensated DAC Output Spectrum.

2.3.2 Need for Further Work

Section 2.3.1 shows that the lowpass calibration technique is not entirely successful, it is necessary to obtain another band of information. By incorporating a higher band of frequencies, the DAC errors that were not present in the lowpass calibration can be captured. By gaining information from this second, higher frequency band, the DAC error characteristic formed will better depict the DAC's actual characteristic. High frequency terms that were left uncompensated from the lowpass calibration can now compensated. It is this concept that leads to the development of this thesis.

The fact that the clock to the ADC was present in the DAC's output and that the noise floor was high (and unrepeatable) also lead to a focus of this thesis. A wire-wrap prototype implementation was used to produce the early results seen in Section 2.3.1. This led to results that were not only unrepeatable due to orientation of different portions of the DAC calibration hardware, but results that were undesirable. For example, the largest distortion term in the DAC output spectrum was the clock that was driving the ADC. These undesirable factors, unrepeatablity and undesired ADC clock feed through, led to the development of a better DAC calibration hardware design. Improved hardware implementation and need for another measurement band motivated the remaining portions of the thesis.

CHAPTER 3

Calibration Hardware Considerations

This chapter describes how a second band of information was obtained and measured to provide an improved DAC error model. This chapter also explains the hardware implementation used to realize the collection of data. Finally, a discussion of the system calibration is described so that the DAC calibration problem can be independent of the distortion introduced by the hardware.

3.1 Obtaining Second Band Measurements

The results of Section 2.3.1 imply that the DAC error estimate obtained from the lowpass measurement is not enough to complete a full band calibration. It is apparent that some of the dynamic errors are not producing energies at low-band. Because of this the error characteristic formed cannot compensate for the high band errors as the calibration routine has not been able to gather information dependent upon these higher frequencies. This presents the need for the second band of frequency measurements. The second band of measurements can be separated from other energies by constructing an ADC bandpass filter at the DAC output, replacing the ADC lowpass filter in Figure 2.6 creating Figure 3.1.

The problem now becomes how to observe the frequency content passed by the bandpass filter. The first system's only requirement was that the lowpass reconstruction filter's bandwidth was completely within the Nyquist band of the ADC clocked at f_s/R. Now, by introducing energies that are outside of the ADC's Nyquist limit, there are some considerations that need to be made concerning the digitizing of the DAC's analog output and how that affects the spectral output of the ADC.

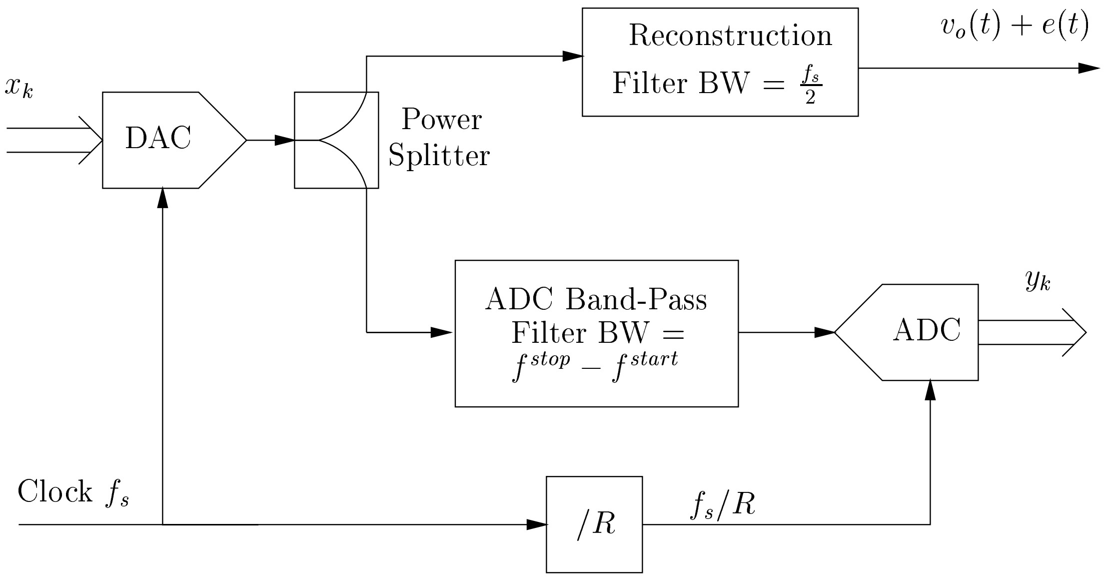

Figure 3.1: Bandpass Calibration System Diagram

3.1.1 Selection of System for Second Band Measurements

There are at least three different ways to be able to digitize a band of information that is of a higher frequency content than the lowpass band. One method would be to use a very high performance ADC capable of sampling fast enough to get accurate representations of higher frequencies. For high-speed DACs, ADCs with adequate resolution are either quite expensive or not available and so other options must be considered. Another method is to use a mixer to translate the desired band down to lower frequencies that would fall into the Nyquist band of the slowly clocked ADC. Another alternative is to use a slow but high resolution ADC with input bandwidth which exceeds its first Nyquist band. For example, input signals which fall into the third ($f_s < f < \frac{3}{2}f_s$) or fourth ($\frac{3}{2}f_s < f < 2f_s$) Nyquist band of the ADC, clock at f_s, can be measured since these bands alias to lower frequencies due to the periodic nature of a sampled spectrum [5]. This is the approach which is pursued in this thesis as the hardware was available to test this concept of using the ADC as a mixer.

To illustrate the measurement of a signal which is not within the first Nyquist band, a simple experiment was conducted. For this example the Analog Devices AD9042D 12-bit ADC was used. A Tektronics 9504 data cache was used to collect N_s = 8k (8k = 8 ∗ 1024 = 8192) samples from the ADC. The HP 9045A signal generator was used to generate a tone in the third Nyquist band of the ADC which was clocked at $f_s = 25.6$ MHz. The specified analog bandwidth of the AD9042D is 100 MHz [1] which allows enough bandwidth for a third Nyquist band test. When performing an ADC test, the selection of an input frequency f_{in} for the test tone is not trivial. With a clever selection for f_{in}, the FFT will provide a Fourier expansion of the input waveform $x(t)$. To accomplish this $x(t)$, should be chosen so that it is periodic with period

$$1/f_o = N_s T_s, \tag{3.1}$$

where

$$T_s = 1/f_s = \text{ sample period.} \tag{3.2}$$

Then, by selecting a frequency f by

$$f = kf_o = k\frac{f_s}{N_s} \qquad \text{for an integer } k, \tag{3.3}$$

ensures a "FFT bin frequency." By selecting a FFT bin frequency the FFT provides an exact expansion separating harmonic components into other frequency bin locations [3]. For example, the first Nyquist band frequency bin numbers of an ADC sampled at f_s using N_s samples are

$$[0,\ 1,\ 2,\ \cdots\ \frac{N_s}{2}]. \tag{3.4}$$

The corresponding frequencies for that band would be

$$[0\frac{f_s}{N_s},\ 1\frac{f_s}{N_s},\ 2\frac{f_s}{N_s},\ \cdots\ \frac{N_s}{2}\frac{f_s}{N_s}] \tag{3.5}$$

through use of equation (3.3). Note that the last term in equation (3.5) simplifies to $f_s/2$, the Nyquist frequency of an ADC sampled at f_s.

In continuation of the third Nyquist test, the input frequency bin $k_i = 8969$ was selected to ensure that the input frequency would fall into the third Nyquist band. Given k_i, calculation of f_{in} can be made

$$f_{in} = k_i \frac{f_s}{N_s} = 28.028125 \text{ MHz}, \tag{3.6}$$

which is certainly in the third Nyquist band. However when collecting ADC output samples, k_i is not the bin number that the FFT of the samples will have. Note that 8969 is greater than $N_s = 8192$. Because of this, the fact that the input frequency is in the third Nyquist band, and due to the periodic nature of the ADC output, by subtracting N_s from k_i, it is possible to obtain the output bin number k_o where

$$k_o = k_i - N_s = 8969 - 8192 = 777. \tag{3.7}$$

The FFT of the ADC output samples for this test is shown in Figure 3.2. This test shows that indeed a frequency introduced in the third Nyquist band of the ADC can be seen at the ADC output, at an aliased FFT frequency bin that can be calculated.

If using this method it is important to know in which of the Nyquist bands the input signal is located since the ADC output reveals no information about which band of frequencies that signal came from. Without that information it would not have been possible to know to subtract N_s in equation (3.7). Since the

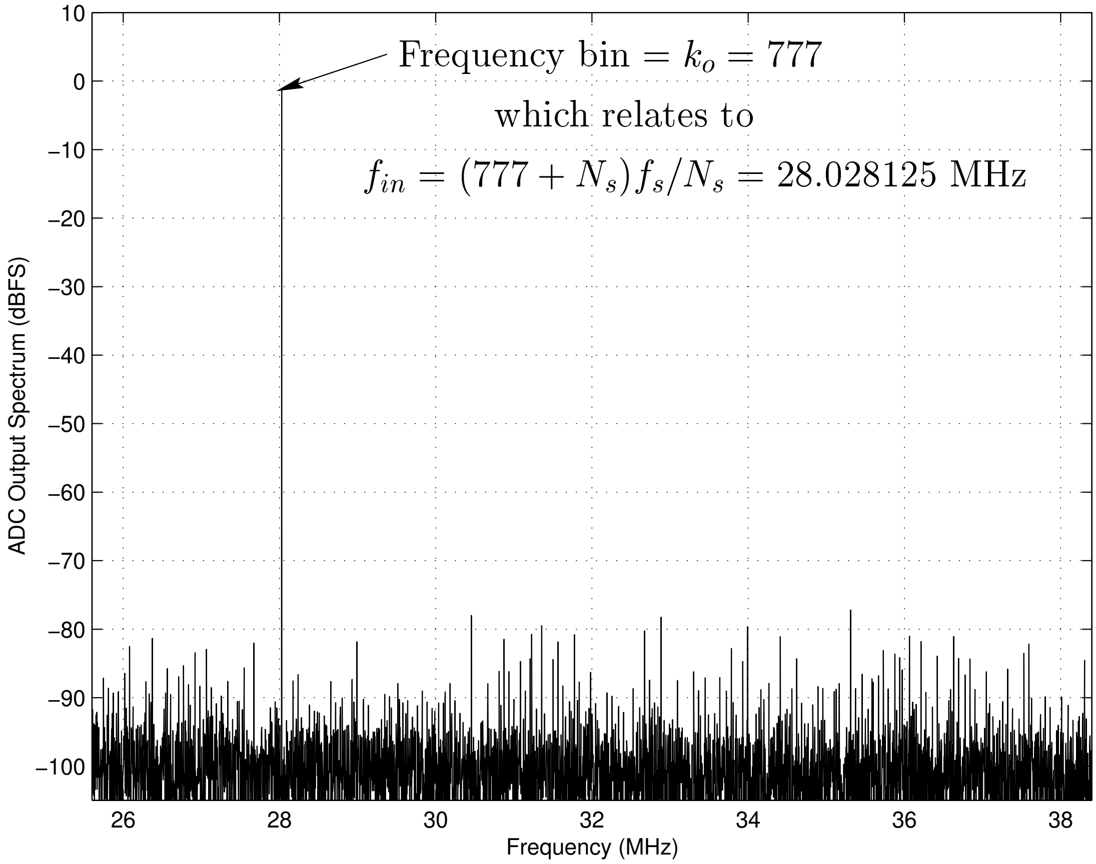

Figure 3.2: ADC Third Nyquist Band Test Spectrum

slowly clocked high resolution ADC can be used as a mixer, it now is necessary to see how frequency bin numbers at the DAC input relate to bin numbers for the ADC output sequence.

3.1.2 DAC to ADC Bin Mapping

The DAC calibration system to obtain a second band of information is shown in Figure 3.1. This is identical to the setup for the lowpass calibration system (Figure 2.6) but the filter has been changed. This will make for an easy transition between obtaining either bands of spectral data. To do this frequency bin mapping which relates the input sample spectrum to the output spectrum must be understood.

Let $\vec{i}_d$ denote the vector of frequency bins that are associated with the passband of the bandpass filter. Note that these are frequency bins with respect to the DAC's sampling frequency and number of samples. For example, with the passband of the filter ranging from $f^{(start)} = 27.3$ MHz to $f^{(stop)} = 34.4$ MHz, the corresponding $\vec{i}_d$ would be determined by calculating the first bin, $i_d^{(start)}$, and last bin, $i_d^{(stop)}$, of $\vec{i}_d$. An example of finding the starting bin is shown in equation (3.8).

$$i_d^{(start)} = f^{(start)} \frac{N_s}{f_s} \tag{3.8}$$

For example, if the number of samples, N_s, is 8k $(8 * 1024)$and the DAC sampling frequency, f_s, is 102.4 MHz, $i_d^{(start)}$ would equal 2184.

The same procedure is used to find the final frequency bin. Once both of these bins have been found, $\vec{i}_d$ would then be filled in by increments of one, starting at the start bin and ending at the stop bin.

$$\vec{i}_d = [i_d^{(start)},\ i_d^{(start)} + 1,\ i_d^{(start)} + 2,\ \cdots,\ i_d^{(stop)}] \tag{3.9}$$

For the example started in equation (3.8), $\vec{i}_d$ would have the values

$$\vec{i}_d = [2184,\ 2185,\ 2186,\ \cdots,\ 2752]. \tag{3.10}$$

$\vec{i}_d$ now represents the DAC input frequency bins that are in the passband of the bandpass filter. Because of this relation to the frequency bins within the bandpass filter the notation $\vec{i}_{dB}$ will be adopted. Similarly, the bins within the passband of the lowpass filter can be calculated, creating the vector of frequency bins, $\vec{i}_{dL}$. With a procedure to determine $\vec{i}_{dB}$ and $\vec{i}_{dL}$, a way to calculate the corresponding ADC output frequency bins, $\vec{i}_{aB}$ and $\vec{i}_{aL}$, will be discussed.

Assume that the number of samples, N_s sent to the DAC will be the same number of samples that will be collected from the ADC. Finding the bin mapping takes a few steps and is started by finding the frequencies, $\vec{f}_{dB}$ that relate to the DAC bins, $\vec{i}_{dB}$.

$$\vec{f}_{dB} = \vec{i}_{dB}\frac{f_s}{N_s} \tag{3.11}$$

Now to see which bins $\vec{f}_{dB}$ relates to in the ADC a similar calculation is made using f_s/R as the sampling frequency of the ADC is used.

$$\vec{i}^{\,*}_{aB} = \vec{f}_{dB}\frac{N_s}{f_s/R} \tag{3.12}$$

Note that equation (3.12) is not an equation depicting the calculation of $\vec{i}_{aB}$ but an intermediate vector $\vec{i}^{\,*}_{aB}$. This is where it is important to understand into which Nyquist band the frequencies of the bandpass filter fall. For continuation of the example started in equation (3.8) assume that $R = 4$, giving an ADC sample frequency of $f_s/R = 25.6$ MHz. It is evident that the frequencies represented in the bins of equation (3.10) would fall into the third Nyquist band of the ADC.

Due to the periodicity of the DFT [5], it is possible to obtain the actual ADC bin numbers, $\vec{i}_{aB}$, from $\vec{i}^*_{aB}$ by subtracting N_s, one period of the ADC. By combining equation (3.11) and equation (3.12) and taking into account the periodicity of the DFT, the mapping between $\vec{i}_{aB}$ and $\vec{i}_{dB}$ is

$$\vec{i}_{aB} = \vec{i}_{dB}R - N_s. \tag{3.13}$$

Please note that this equation is only valid if the number of samples sent to the DAC and received from the ADC are equivalent and if the entire band of the bandpass filter resides in the third Nyquist band of the ADC. It is also important to realize that the bin mapping for the lowpass calibration technique is quite similar. Since the lowpass calibration has all of the frequencies within the first Nyquist band of the ADC it is not necessary to subtract N_s as is done in equation (3.13). The lowpass bins, $\vec{i}_{aL}$, are calculated

$$\vec{i}_{aL} = \vec{i}_{dL}R. \tag{3.14}$$

3.2 Hardware Implementation

With the understanding of how the ADC and DAC bins are related, a discussion of the hardware implementation must be made. This discussion describes how the hardware was realized to accomplish the collection of a second band of information.

The hardware implementation consists of parts shown in Figure 3.3. Note that for the lowpass calibration, the hardware setup is identical except the bandpass filter is replaced with a lowpass filter. The blocks of the system are described below:

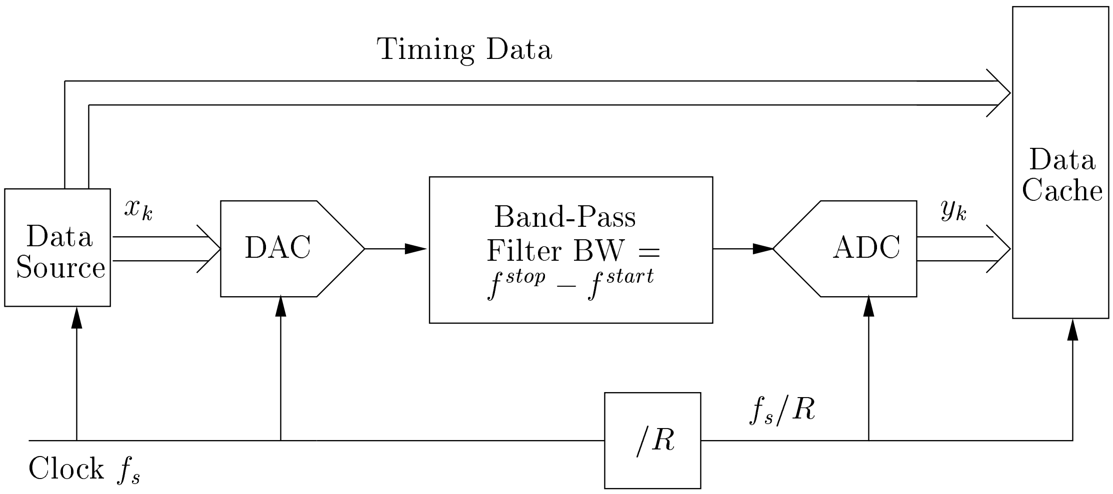

Figure 3.3: DAC Calibration Hardware Block Diagram

1. Data Source: Hewlett Packard HP16522A pattern generator.
2. DAC: Maxim 555, 12-bit 300 MSPS DAC
3. Band-Pass Filter: 5^{th} order elliptical bandpass filter
4. ADC: Analog Devices AD9042D 12-bit ADC
5. Data Cache: Tektronics 9504 Fast Data Cache
6. $/R$: Clock Division Circuitry

This listing is identical to the components used in [6] except for the change of filter and the Maxim 555 replacing the Tektronics TKDA30P.

The filter is an elliptical, fifth order, bandpass filter built on a two layer printed circuit board layout. This layout was composed using a software program, called PCB (version 1.6.3), by undergraduate student Scott Saucier. This program had the proper output format, RS-247 Gerber X, required by many manufacturers for fabrication.

Filter Spec.	Value
Filter Order	5^{th}
f^{start}	27.3 MHz
f^{stop}	34.4 MHz
Passband Ripple	1 dB
Stopband Attenuation	60 dB

Table 3.1: Bandpass Filter Specification Table

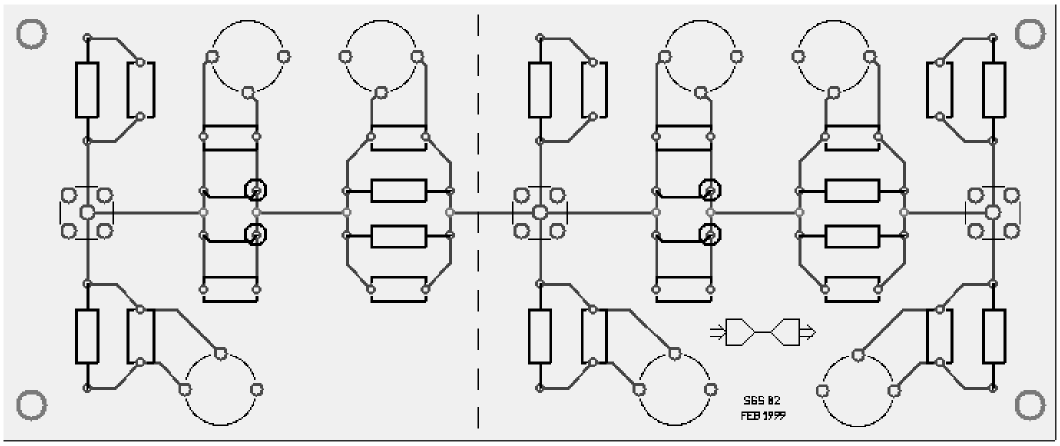

Figure 3.4: PCB Filter Layout

Mr. Saucier derived the element values to create a fifth order elliptical filter with specifications shown in Table 3.1. The PCB layout of the filter is shown in Figure 3.4.

Using the same software package, Mr. Saucier also constructed a layout for the Maxim 555 12 bit DAC. This board not only held the appropriate DAC circuitry but also held the clock divide circuit (a series of flip-flops) to obtain the $/R$ clock for the ADC and a circuit that interfaced the ADC output to the data cache. An example of the layout can be seen in Figure 3.5. The purpose of this setup was to obtain a better ground plane reference to provide repeatability of experiments and to hopefully reduce the clock feed-through, observed in Figure 2.8.

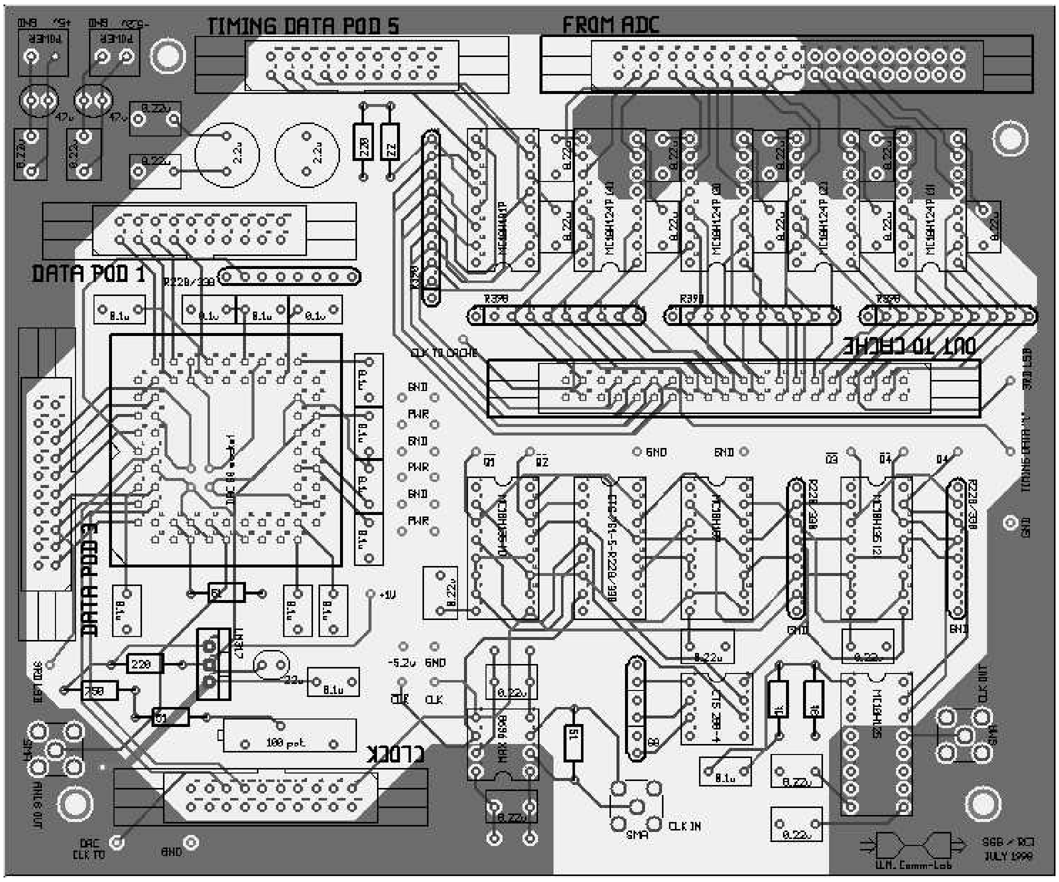

Figure 3.5: PCB DAC Layout

After designing the board, ensuring that all traces needed were there, sending the design for fabrication, and finally soldering every piece onto the layout, it was time to test the DAC setup. Originally the Tektronics DAC was still being used but it was soon realized that an improper reference current was being delivered. A voltage reference and a internal resistance were being used by the original DAC. When it was decided to use a current reference for the DAC due to grounding problems with the voltage reference setup, it was noticed that the Tektronics DAC no longer had the internal resistance necessary to help control the current reference. When using the voltage reference, which relied on the internal resistance, the Tektronics DAC was being supplied twice the reference current than was specified. This led to the purchase of the Maxim part, which is a pin-for-pin replacement for the Tektronics part, and the inclusion of the current reference to ensure the proper reference level.

A disturbing problem was associated with the clock generated by the HP pattern generator. Originally the pattern generator had provided the clock to the DAC. This was a nice feature as the clock from the pattern generator could be manipulated to align perfectly with the data being handed to the DAC. However, examination of the quality of the clock generated by the data source revealed undesirable results. The pattern generator had internal dividing circuitry which corrupted the clock output. No matter how spectrally pure the clock handed to the pattern generator, it would return a clock that had harmonics that would introduce errors in the DAC output. To combat this problem a separate comparator was used to provide a clean clock the the DAC. Unfortunately this clock was not lined up with the data from the pattern generator. To achieve this alignment a length of transmission line is used to approximate the delay the pattern generator introduces.

The above changes produced significant improvement in the DAC spectral output as seen in Figure 3.6. Note that the clock spike is no longer present and

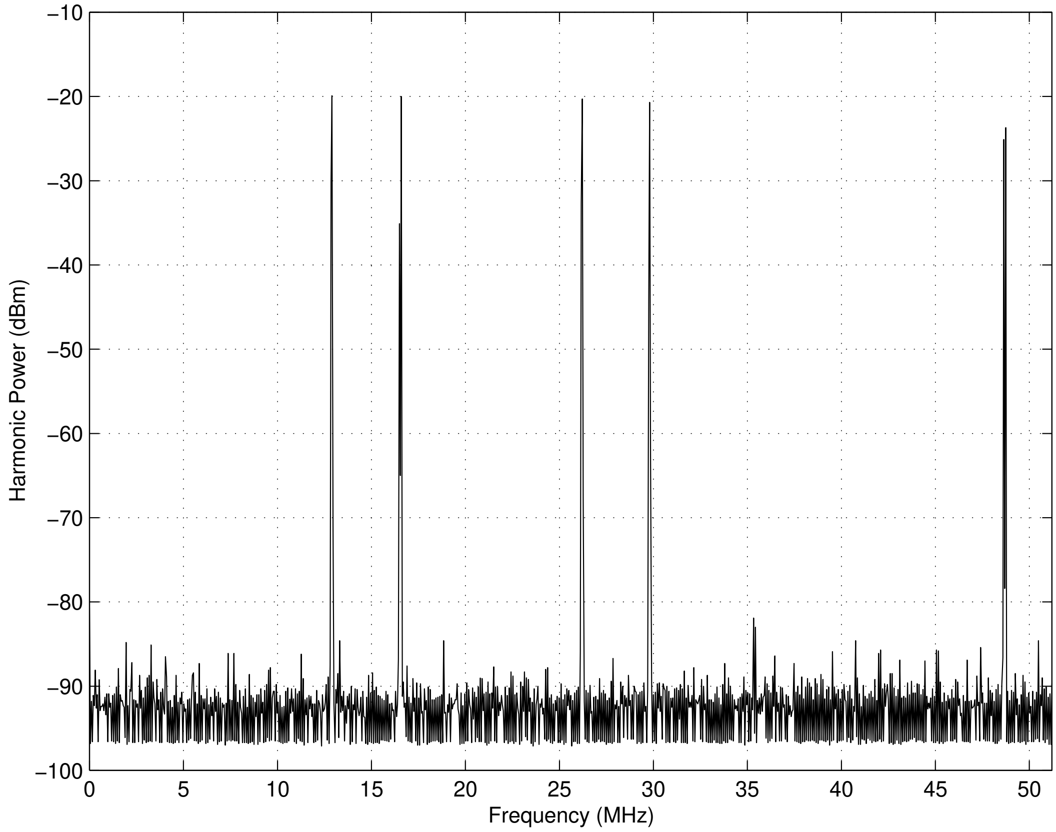

Figure 3.6: PCB Hardware Output Spectrum Test

that the noise floor is considerably lower. Also, the results of the new setup are independent of how particular pieces of the setup may be oriented. The old setup required much effort to achieve an output that looked reasonable. Now the setup provides results that are not only spectrally clean but also repeatable.

3.3 System Calibration

Upon inspection of Figure 3.3 one can see the inclusion of timing data which is not present in previous figures of the calibration setup. The data source is generating a timing sequence, along with the DAC samples, and handing the timing data to the data cache. This inclusion of timing data allows for a delay normalization to help account for delay that the hardware implementation introduces between the DAC input and the ADC output samples. It is important to have a linear characterization of the system which allows the calibration routine to measure DAC errors and not gain and phase changes added by the signal path.

3.3.1 Delay Normalization

In order to make meaningful phase measurements of the data received by the cache it is important to employ a delay normalization. In effect, the samples sent to the DAC and the sample received from the ADC need to be aligned in time. This is the reason for the timing data the data source creates and sends to the data cache, as included in Figure 3.3. The timing data are created in a manner allowing the delay normalization to be accomplished.

In determining the timing data sequence it is important to know what the clock divide factor, R, is. Since ADC is clocked at a slower rate, f_s/R, a calculation of a fractional delay becomes necessary. The timing sequence sent is N_s samples long, the same length as the samples sent to the DAC. The start and ending of the sequence is dependent on R as the data held in these positions must cover enough length so that the slowly clocked ADC will receive a position of the timing sequence. This sequence is best seen in an example. Assume R to be four and N_s to be 8k (8192). This N_s long sequence is sent out at frequency f_s. The data cache collects samples at f_s/R, the clock rate used by the ADC. Since the cache is basically receiving every fourth sample, $\vec{t_s}$ is constructed

$$\vec{t_s} = [0\ 1\ 2\ 3\ 0\ 0\ \cdots\ 0\ 0\ 1\ 1\ 1\ 1]. \tag{3.15}$$

If R had been eight, $\vec{t_s}$ would have started with $[0\ 1\ 2\ \cdots\ 6\ 7]$ and ended with a series of eight ones. This timing information must have enough length to cover the clock divide factor, R. The received sequence, $\vec{t_r}$, has the form

$$\vec{t_r} = [0\ 0\ 0\ \cdots\ 0\ 1\ L\ 0\ 0\ \cdots] \tag{3.16}$$

where L is an integer ranging from 0 to $R-1$. The entire form of $\vec{t_r}$ will actually be every fourth sample of $\vec{t_s}$, starting at any random location in $\vec{t_s}$, and then repeated four times to form $\vec{t_r}$. Since the DAC data source and ADC collection are not synchronized, it is not known where the 1 and L will first fall in $\vec{t_r}$. But the information necessary to calculate the fractional delay is present in the portion shown in (3.16).

To make use of the timing data, two things need to be derived from $\vec{t_r}$; the position where the first "1" falls, Q, and the value of L. Q is then interpreted as the number of full (ADC) sample delays of the DAC sequence with the collected buffer and L is a fractional delay. The delay normalization may be applied in the frequency domain, which is convenient since the DAC error is being observed in the frequency domain. The transform pair for a integer delay, n_d, is

$$x[n - n_d] \Longleftrightarrow e^{-j2\pi n_d \frac{n}{N_S}} X_n. \tag{3.17}$$

The delay, n_d, will have a form which represents the amount of delay between the time of the sent DAC samples and the received cache samples, calculated from Q and L. This leads to

$$d_i = e^{j2\pi(Q-L/R)\frac{i+N_s}{N_s}}, \tag{3.18}$$

where d_i represents the delay to be applied to frequency bin i, of the received samples.

One interesting note to make is the $i + N_s$ factor in equation (3.18). The addition of N_s is present due to the fact that the bandpass calibration is being done in the third Nyquist band of the ADC. For the lowpass calibration, N_s would not be added to frequency bin number i in calculation of d_i. It should also be noted that equation (3.18) only holds for the positive frequency bins. Which bins represent positive and negative frequencies must be distinguished as the FFT returns both. For the FFT frequency bins which correspond to the negative frequencies, the conjugate of equation (3.18) must be used. Multiplying the d_i factor by the corresponding frequency bin of the received cache samples provides a consistent phase reference. Because of this, any further discussion of received cache samples will be assumed to have the delay normalization applied.

With a method developed to normalize the delay for the received data from the ADC for both the lowpass and second band calibration techniques, the calibration system delays can be eliminated from the collection of data. However, before the calibration hardware discussion can end, a linear characterization of the calibration system must be developed.

3.3.2 Linear Characterization

In the calibration scheme it is important to have a set of gains which represents the gain and phase changes made to the signal throughout the path of the system. The filter, whether a lowpass or bandpass, will add gains and delays as well as the pipeline delays found in the DAC and ADC. With the calculation of a linear characterization, development of a mathematical model for the DAC errors becomes possible.

The goal here is to produce a vector, $\vec{G}$, where G_{i_d} will be the gains associated with frequency bin i_d in the band of interest. i_d will have values to cover every bin in the passband (whether lowpass or bandpass) of the filter. By obtaining the Fourier Transform of the input samples, $\vec{X}$, and the received cache output samples, $\vec{Y}$, it is possible to calculate the gains for every bin, i_d, in the band of interest. This is accomplished by introducing a pure cosine in every frequency bin i in the passband of the filter and comparing the input samples to the received output samples. For bin i_d, G_{i_d} is calculated

$$G_{i_d} = \frac{Y_{i_a}}{X_{i_d}}. \tag{3.19}$$

Where i_a will either be i_{aL} or i_{aB} depending on whether the lowpass or bandpass calibration is being used. The derivations of i_{aL} and i_{aB} are found in Section 3.1. This process is completed by introducing pure cosines for every bin i in the passband of the filter and saving the G_i's in $\vec{G}$. $\vec{G}$ is then saved for future use in the calibration routine.

With the completion of the linear calibration the hardware setup has been entirely removed from considerations of calibration technique. The delay normalization ensures that output samples received from the cache will maintain a consistent phase reference. Using the linear calibration, the ADC output can be used to measure the DAC error without being influenced by the gain and phase changes introduced by the linear portion of the calibration system.

CHAPTER 4

Multi-Band Calibration Technique

This chapter explains the theory behind the basis function representation of the DAC error and provides improvements over previous calibration techniques. These improvements include the calibration signal selection and methods of calculation of basis function weights. Finally this chapter provides a step-by-step two-band DAC calibration overview.

4.1 Basis Function Representation

The problem of DAC calibration now turns to the problem of estimation of the error function $e(x_k, x_{k-1})$ developed in Section 2.1.3. A common method of approximating unknown functions is by the use of basis functions. With the use of known basis functions it becomes possible to approximate an unknown function with the use of a finite number of coefficients (or weights) and basis functions. In this thesis the basis functions are chosen to be a function of the current input code and previous input code to match the measured error function. Each basis function, $b_j(x_k, x_{k-1})$, has a corresponding weight, w_j. For N_b specified basis functions, there will be N_b w_j's to be determined. It is this calculation of the w_j's that becomes a challenge in the use of basis functions for function approximation. The estimate of the error function, $\hat{e}(x_k, x_{k-1})$, using N_b basis functions and weights is formed by

$$\hat{e}(x_k, x_{k-1}) = \sum_{j=1}^{N_b} w_j b_j(x_k, x_{k-1}). \tag{4.1}$$

For a given current input sequence

$$\vec{x}_k = \left[\begin{array}{ccccc} x_1 & x_2 & x_3 & \dots & x_N \end{array} \right] \tag{4.2}$$

and its associated previous input sequence

$$\vec{x}_{k-1} = \left[\begin{array}{ccccc} x_N & x_1 & x_2 & \dots & x_{N-1} \end{array} \right] \tag{4.3}$$

both length N, equation (4.1) produces N equations to be used to solve for the w_j's. However the summation notation is not convenient for a common method of solving for appropriate weights. Here a least-square solution [7] is used to solve for the w_j's. It is convenient to adopt a vector notation. The set of N equations from (4.1) can be written in the matrix form

$$\hat{\vec{e}} = \tilde{b}\vec{w}, \tag{4.4}$$

with $\hat{\vec{e}}$ defined as

$$\hat{\vec{e}} = \left[\begin{array}{c} \hat{e}(x_1, x_N) \\ \hat{e}(x_2, x_1) \\ \vdots \\ \hat{e}(x_N, x_{N-1}) \end{array} \right], \tag{4.5}$$

$\tilde{b}$ defined as

$$\tilde{b} = \begin{bmatrix} b_1(x_1, x_N) & b_2(x_1, x_N) & \dots & b_{N_b}(x_1, x_N) \\ b_1(x_2, x_1) & b_2(x_2, x_1) & \dots & b_{N_b}(x_2, x_1) \\ b_1(x_3, x_2) & b_2(x_3, x_2) & \dots & b_{N_b}(x_3, x_2) \\ \vdots & \vdots & \ddots & \vdots \\ b_1(x_N, x_{N-1}) & b_2(x_N, x_{N-1}) & \dots & b_{N_b}(x_N, x_{N-1}) \end{bmatrix}, \tag{4.6}$$

and $\vec{w}$ defined as

$$\vec{w} = \begin{bmatrix} w_1 \\ w_2 \\ \vdots \\ w_{N_b} \end{bmatrix}. \tag{4.7}$$

Gaussian basis functions are used in this thesis. Basis function b_j has the form

$$b_j(x_k, x_{k-1}) = e^{-\frac{1}{2\sigma^2}((\vec{x}-\vec{c}_j)^T(\vec{x}-\vec{c}_j))}. \tag{4.8}$$

With centers

$$\vec{c}_j = \begin{bmatrix} c_j^{(1)} & c_j^{(2)} \end{bmatrix}^T, \tag{4.9}$$

and input samples

$$\vec{x} = \begin{bmatrix} x_k & x_{k-1} \end{bmatrix}^T. \tag{4.10}$$

To make use of the basis functions, an intelligent selection of $\vec{c}_j$'s and σ^2 must be made. The centers were chosen to be evenly spaced in the input space of current - previous input. A grid of 100 centers was used as shown in Figure 4.1.

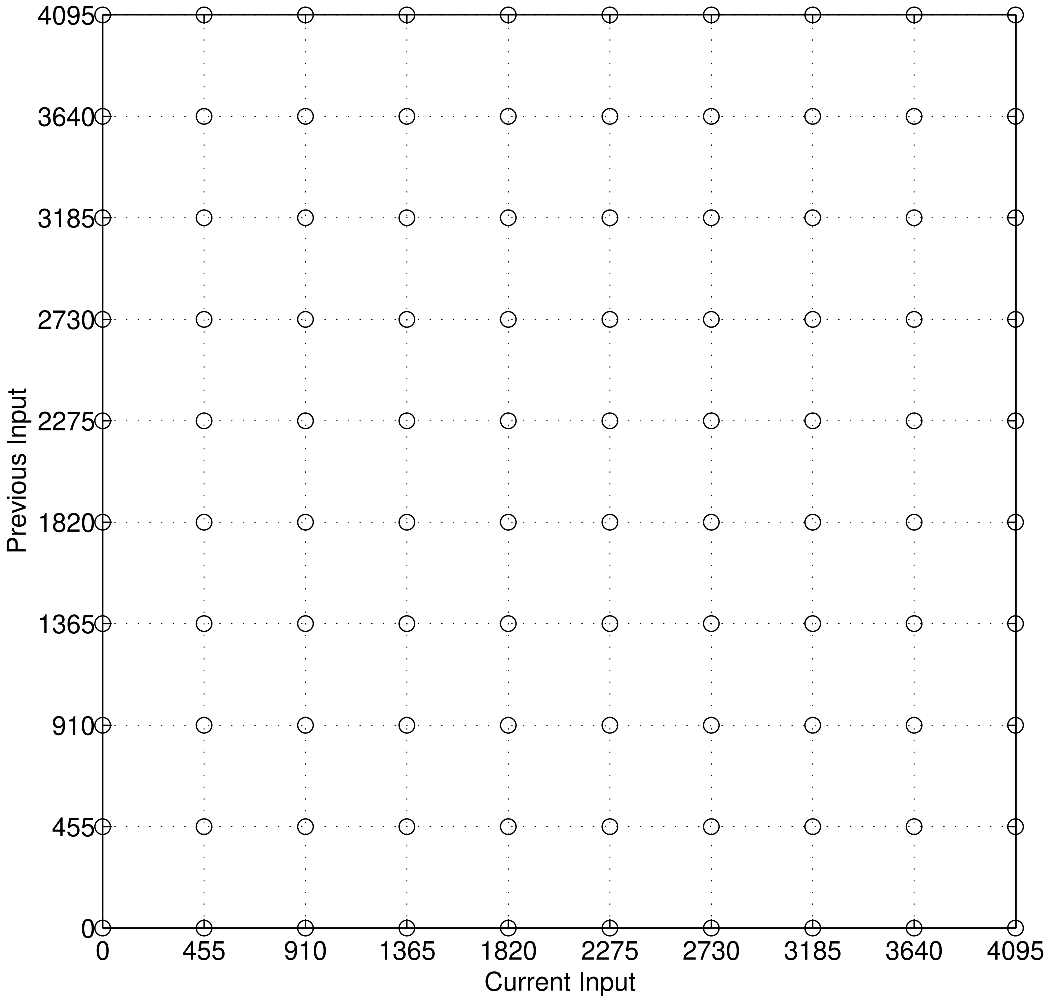

Figure 4.1: Plot of 100 Basis Function Centers for a 12-bit DAC

σ is chosen as

$$\sigma^2 = \frac{d^2}{2} = 103512.5, \tag{4.11}$$

where

$$d = \text{ distance between closest Centers.} \tag{4.12}$$

These definitions created the 100 basis functions used throughout the thesis.

4.2 Calibration Signal Selection

To properly determine the error characteristic for the DAC, the input space for the set of basis functions needs to be filled. The input space for this problem is the current input - previous input state space. For this space to be filled, many combinations of current input and previous inputs must be hit. Previously a set of five tone input signals were used to completely cover the current input - previous state space as shown in Figure 4.2 [6]. Figure 4.2 was created by using 100, five-tone signals. This is a very time consuming and undesirable practice in state space filling.

After studying how different input frequencies affect the basis function input space, it was determined that one multi-tone signal could be used to cover this space effectively. For example, lower frequency terms fill the input space for small changes between a current input and its previous input. Conversely, higher frequency terms fill the input space for large changes. Middle frequency terms fill the middle of the the input space.

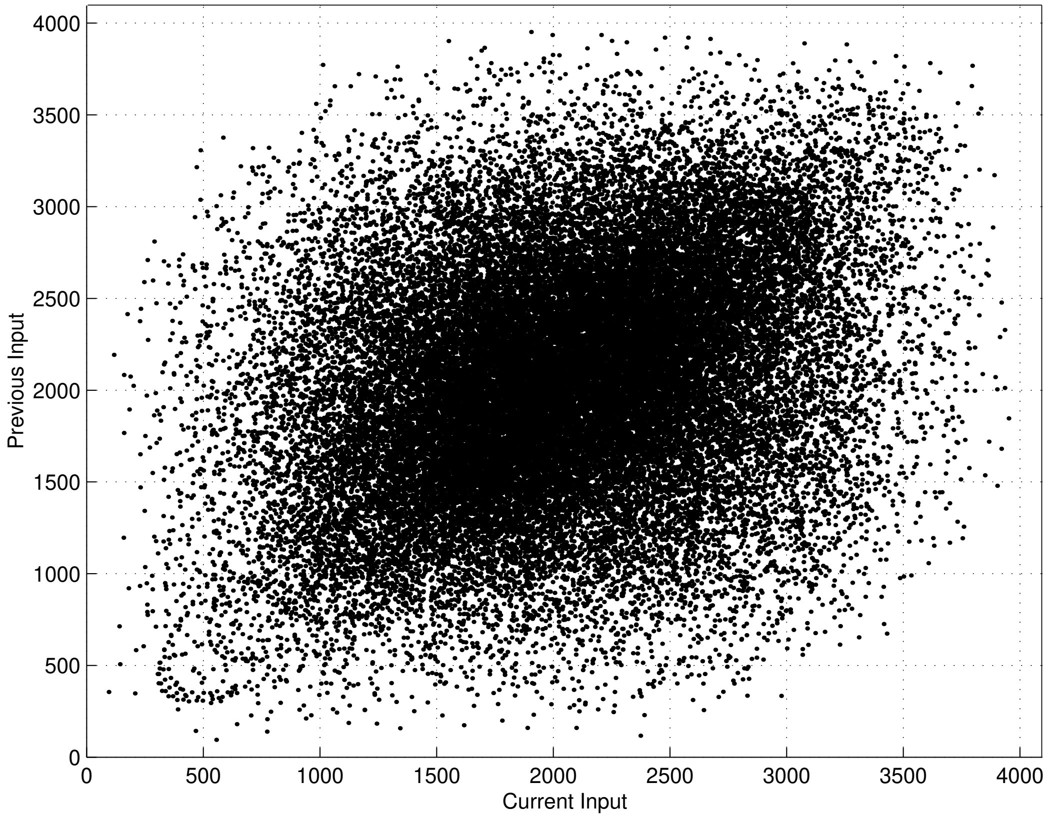

Figure 4.2: 100 Multi-Tone Basis Function Input Space

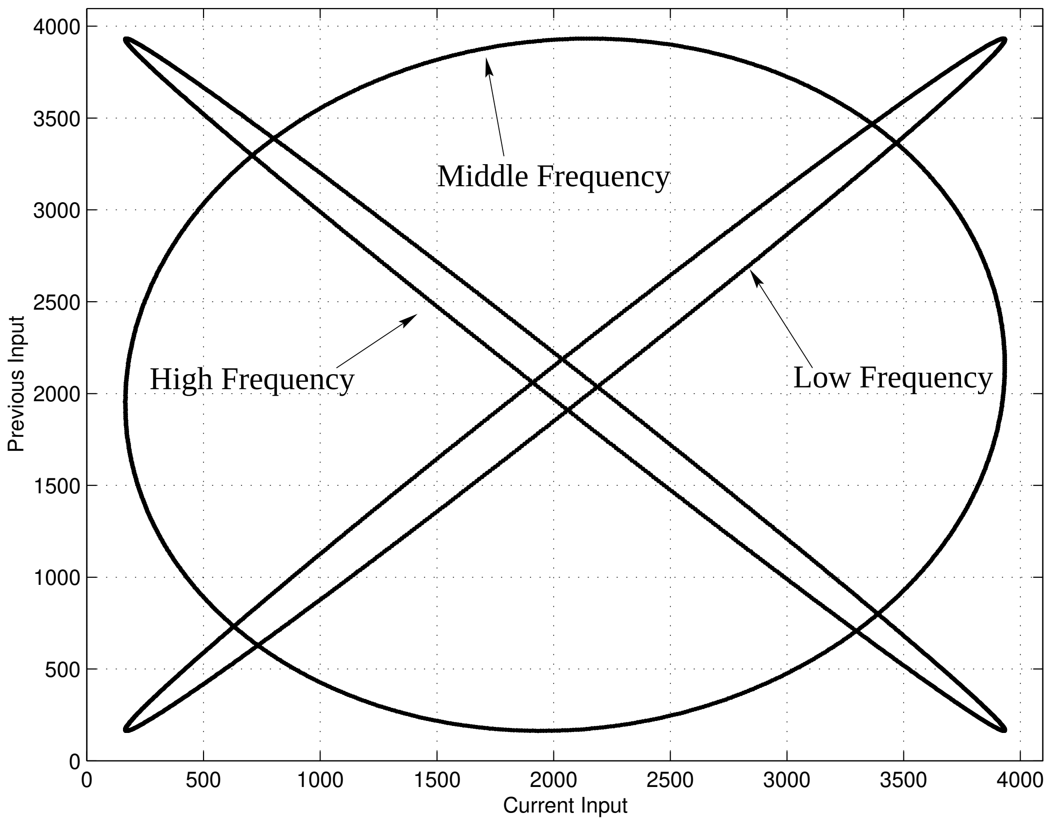

Figure 4.3: State Space Filling Curves

The current input - previous input space for three separate sinusoids with different frequencies is illustrated in Figure 4.3. This figure was created by using three separate single tone inputs (high, low, and middle frequencies).

In observing the input space filling response due to different frequencies, one can see that tones selected across the frequency band should be a good selection. A six tone input signal was selected to cover the input space. After some experimentation with variations in the amplitude and phase of each tone, a scheme was realized to produce a well covered input space. By choosing the six tones to have amplitudes which are nearly equal but phases that are distributed quadratically, a desirable input space was found with parameters listed in Table 4.1 This signal's input space is illustrated in Figure 4.4.

Tone #	FFT Bin #	Nominal Amplitude (LSBs)	Phase (rad)
1	101	530	0
2	880	530	1.5080
3	1659	530	2.2619
4	2439	530	2.2619
5	3218	530	1.5080
6	3997	530	0

- FFT bin numbers assume $N = 8192$ points in the sequence.
- Actual amplitudes are varied randomly by ± 10 LSBs.

Table 4.1: Six Tone Calibration Signal Parameter Table.

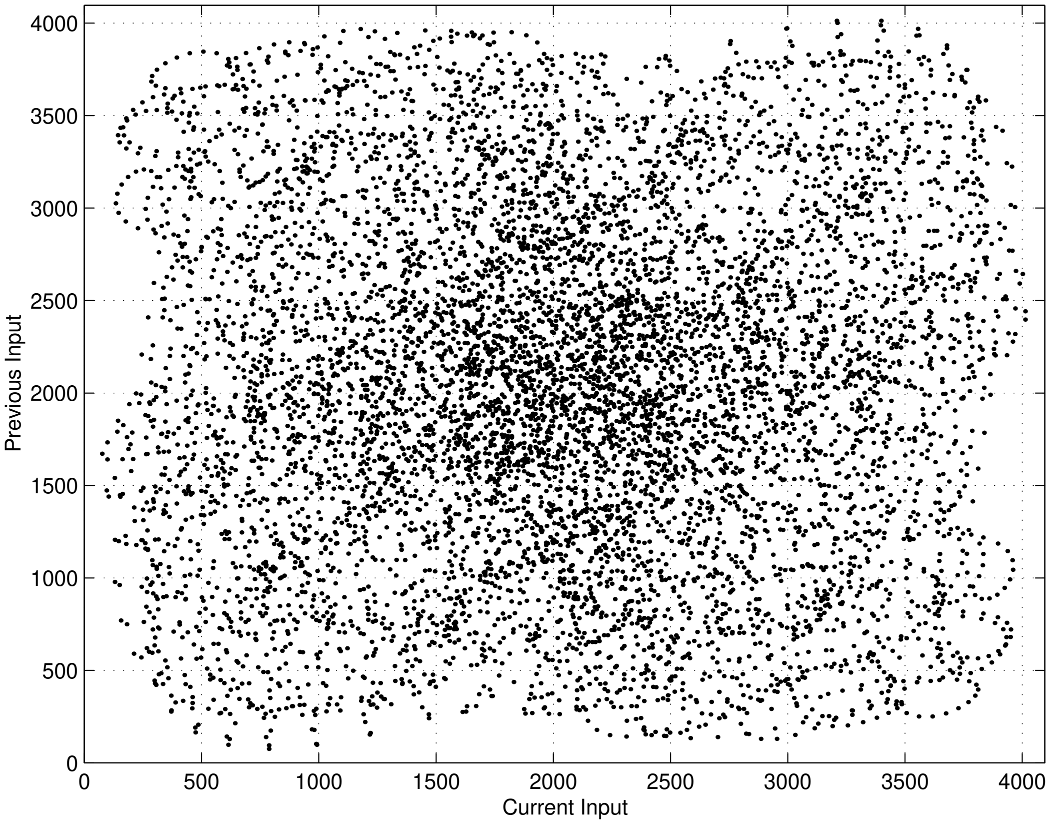

Figure 4.4: One Multi-Tone Input Space

This six-tone signal will be used in calibration of the DAC. Since the input covers many current input - previous input combinations, the six tone input signal should be a good choice for a single calibration signal. By using the selected input signal the time needed to calculate the basis function weights is reduced dramatically as the time needed by the pattern generator to create a single sequence is quite long.

4.3 Calculation of Basis Function Weights

Recall the DAC error model ϵ_k introduced in Section 2.1.3. Then, $\vec{\epsilon}$ is defined as the unknown error function for the determined calibration input sequence. Due to the limitations of the calibration system, $\vec{\epsilon}$ cannot be measured. However, certain frequency domain intermodulation distortion terms do fall into the calibration band. The measured frequency error terms created by the Fourier transform matrix

$$\vec{\mathcal{E}} = \tilde{T}\vec{\epsilon} \tag{4.13}$$

are manipulated to find an equation which can be solved for $\vec{w}$. The procedure is explained below.

1. Send the calibration input sequence $\vec{x}$ to the DAC. This signal is assumed to contain a small number of fundamental tones so that its FFT possesses energy in only a small number of "fundamental bins".

2. Collect the ADC output samples $\vec{y}$.

3. Use selected rows of the Fourier transform matrix $\tilde{T}$ (using indices $\vec{i}_{aB}$ or $\vec{i}_{aL}$ from Section 3.1) to obtain frequency components in the measurement bands, either the bandpass or lowpass band.

$$\vec{Y}^b = \tilde{T}_{\vec{i}_{aB}}\vec{y} \;\text{ or }\; \vec{Y}^l = \tilde{T}_{\vec{i}_{aL}}\vec{y} \tag{4.14}$$

4. For a non-fundamental DAC input bin i_d (and corresponding ADC output bin i_a) the measured error power $\mathcal{E}_{i_d}$ can be calculated from the ADC output coefficient Y_{i_a} and the DAC input coefficientX_{i_d}

$$\mathcal{E}_{i_d} = Y_{i_a}/G_{i_d} - X_{i_d}, \tag{4.15}$$

where

$$G_{i_d} = \text{ calculated and stored linear gain for DAC input bin } i_d, \tag{4.16}$$

and

$$X_{i_d} = 0, \tag{4.17}$$

because the DAC input sequence will have no power in a non-fundamental bin. For a set of measurement bins $\vec{i}_d$ this gives

$$\tilde{T}_{\vec{i}_d}\vec{\epsilon} = \vec{\mathcal{E}}_{\vec{i}_d} = \tilde{G}^{-1}\vec{Y}_{\vec{i}_a} = \tilde{G}^{-1}\tilde{T}_{\vec{i}_a}\vec{y}. \tag{4.18}$$

$\vec{\mathcal{E}}_{\vec{i}_d}$ is the vector of measurement errors for a measurement band and $\tilde{G}$ is a diagonal matrix with diagonal elements given by the gains for each bin in the measurement band. Note that $\tilde{G}^{-1}\tilde{T}_{\vec{i}_a}\vec{y}$ is known.

5. Finally an equation can be formed to find a $\vec{w}$ so that $\tilde{T}\hat{\vec{e}}$ (or $\tilde{T}\tilde{b}\vec{w}$) agrees with measured values $\tilde{T}\vec{\epsilon}$

$$\tilde{G}^{-1}\tilde{T}_{\vec{i}_a}\vec{y} = \tilde{T}_{\vec{i}_d}\tilde{b}\vec{w} + \vec{\gamma} = \vec{\mathcal{E}}_{\vec{i}_d}, \tag{4.19}$$

or more simply written

$$\vec{\mathcal{E}}_{\vec{i}_d} = \tilde{B}_{\vec{i}_d}\vec{w} + \vec{\gamma}. \tag{4.20}$$

where $\vec{\gamma}$ is the vector of residual modeling error for the measurement band.

6. To calculate weights which produces the most accurate error sequence, the real and imaginary parts of $\vec{\mathcal{E}}_{\vec{i}_d}$ and $\tilde{B}_{\vec{i}_d}$ are separated

$$\begin{bmatrix} \Re\left(\vec{\mathcal{E}}_{\vec{i}_d}\right) \\ \Im\left(\vec{\mathcal{E}}_{\vec{i}_d}\right) \end{bmatrix} = \begin{bmatrix} \Re\left(\tilde{B}_{\vec{i}_d}\right) \\ \Im\left(\tilde{B}_{\vec{i}_d}\right) \end{bmatrix} \vec{w} + \begin{bmatrix} \Re\left(\vec{\gamma}\right) \\ \Im\left(\vec{\gamma}\right) \end{bmatrix}, \tag{4.21}$$

7. Equation (4.21) represents the error for every non-fundamental DAC input bin. The formulation so far produces an unconstrained solution for $\vec{w}$ which could introduce a linear component in the solution. To combat this effect the gain of the system is controlled by adding two equations to the system. This is done by setting the measured error for a fundamental bin k equal to zero and rewriting equation (4.21)

$$\begin{bmatrix} \Re\left(\vec{\mathcal{E}}_{\vec{i}_d}\right) \\ 0 \\ \Im\left(\vec{\mathcal{E}}_{\vec{i}_d}\right) \\ 0 \end{bmatrix} = \begin{bmatrix} \Re\left(\tilde{B}_{\vec{i}_d}\right) \\ \Re\left(\vec{B}_k\right) \\ \Im\left(\tilde{B}_{\vec{i}_d}\right) \\ \Im\left(\vec{B}_k\right) \end{bmatrix} \vec{w} + \begin{bmatrix} \Re\left(\vec{\gamma}\right) \\ 0 \\ \Im\left(\vec{\gamma}\right) \\ 0 \end{bmatrix}, \tag{4.22}$$

which is rewritten

$$\vec{\mathcal{E}}_t = \tilde{B}_t \vec{w} + \vec{\gamma}_t, \tag{4.23}$$

where the subscript t represents the total information included within the measurement band. It is equation (4.23) that is solved to find $\vec{w}$.

$\vec{w}$ is selected to minimize the sum of the squares of the residual modeling error

$$\vec{\gamma}_t^T \vec{\gamma}_t = \left(\vec{\mathcal{E}}_t - \tilde{B}_t \vec{w}\right)^T \left(\vec{\mathcal{E}}_t - (\tilde{B}_t \vec{w}\right). \tag{4.24}$$

This is done with a least-squares solution [7] providing

$$\vec{w} = \left[\tilde{B}_t^T \tilde{B}_t\right]^{-1} \tilde{B}_t^T \vec{\mathcal{E}}_t \tag{4.25}$$

It should be noted that this pseudo inverse solution is for one measurement band. This thesis investigates a multi-band technique requiring the need to produce a solution for two bands of measurement. Fortunately, due to the construction of the pseudo inverse matrices ($\tilde{B}^T \tilde{B}$ and $\tilde{B}^T \vec{\mathcal{E}}$), the additional measurements are simply introduced to this solution by

$$\vec{w} = \left[\ \tilde{B}_{tB}^T \tilde{B}_{tB} + \tilde{B}_{tL}^T \tilde{B}_{tL}\ \right]^{-1} \left[\ \tilde{B}_{tB}^T \vec{\mathcal{E}}_{tB} + \tilde{B}_{tL}^T \vec{\mathcal{E}}_{tL}\ \right], \tag{4.26}$$

where the subscripts tB and tL represent the total information included in the bandpass measurement and lowpass measurement, respectively.

For ease of notation, equation (4.26) adopts the notation

$$\vec{w} = \tilde{\mathbf{B}}^{-1}\vec{\mathbf{E}}. \tag{4.27}$$

The possibility that $\tilde{\mathbf{B}}$ may be singular drives the need to use another method of solving the matrix inverse.

4.3.1 Singular Value Decomposition for Weight Calculation

If $\tilde{\mathbf{B}}$ is singular, or nearly singular, numerically unstable results will be obtained for $\vec{w}$. To avoid this problem a Singular Value Decomposition (SVD) technique can be employed. SVD is a method used to avoid taking matrix inverses of a matrix that is nearly singular. Here, the modified basis function output matrix, $\tilde{\mathbf{B}}$ has dimensions N_b by N_b, (N_b being number of basis functions) matrix. The first step is to apply the SVD operator to the matrix $\tilde{\mathbf{B}}$ giving

$$\tilde{\mathbf{B}} = \tilde{U}\tilde{S}\tilde{V}^T. \tag{4.28}$$

Here $\tilde{U}$ (an N_b by N_b matrix) is the left singular vectors of $\tilde{\mathbf{B}}$, and $\tilde{V}$ (a N_b by N_b matrix) is the right singular vectors of $\tilde{\mathbf{B}}$. $\tilde{S}$ (a N_b by N_b matrix) is a diagonal matrix with the diagonal terms being the square root of the eigenvalues of $\tilde{\mathbf{B}}^T\tilde{\mathbf{B}}$. Since $\tilde{\mathbf{B}}$ is symmetric, U and V will be equivalent and the diagonal terms of $\tilde{S}$ are the eigenvalues of $\tilde{\mathbf{B}}$ [7]. Also, due to the construction of V

$$VV^T = I \quad \text{or} \quad V^{-1} = V. \tag{4.29}$$

Because of this fact an equivalent system can be found, seen in equation (4.30).

$$\vec{w} = \tilde{V}\tilde{S}^{-1}\tilde{U}^T\vec{\mathbf{E}} \tag{4.30}$$

The matrix equation (4.30) can be rewritten as a summation

$$\vec{w} = \sum_{j=1}^{N} \frac{1}{\sigma_j}\vec{V}_j\vec{U}_j^T\vec{\mathbf{E}}, \tag{4.31}$$

where $\frac{1}{\sigma_j}$ is the jth diagonal value of $\vec{S}$, $\vec{V}_j$ is the jth column of $\tilde{V}$, and $\vec{U}_j$ is the jth column of $\tilde{U}$. N_b is the same variable that was used in defining the matrix dimensions of the SVD matrices. As this thesis makes use of 100 basis functions, N_b becomes equal to 100.

Equation (4.31) indicates the problem if $\tilde{\mathbf{B}}$ is near singular. If the values of $\frac{1}{\sigma_j}$ become small, the summation becomes numerically unstable and $\vec{w}$ takes on large values. To avoid this, the summation can be terminated at

$$D \leq N_b. \tag{4.32}$$

Unfortunately it is a difficult problem to determine a limit on $\frac{1}{\sigma_j}$ which would then set D. In this thesis D was determined by examining the compensated output spectrum. Since the compensated output, whether a simulated or a real system, is not discussed until Section 5.1.1, the actual selection of D will discussed later. Section (5.1.1) examines the improvement of the output using different values for D.

4.4 Input Sequence Compensation

With $\vec{w}$ determined it is possible to compensate a random input sequence. The compensated DAC input $\vec{x}_c$ could be determined using an iterative procedure as described in Section 2.2 [6]. This is the approach the previous DAC compensation attempt used. This may be a valid approach but it can cause problems. In practice, depending on the value of $\vec{w}$, the iterative procedure may or may not converge.

This thesis uses a simpler approximation which gave better performance. With $\vec{w}$ determined, there will be an estimated error $\hat{e}_k$ for every DAC input code x_k. By subtracting these two values a compensated code x_{c_k} can be obtained. The assumption which makes x_{c_k} a valid solution is that the error introduced by the uncompensated sequence x_k and the error introduced by the compensated sequence x_{c_k} are approximately equal. With this assumption, the error model introduced in Section 2.1.3 will provide the desired output. This is a good approximation for the smooth Gaussian functions used. The compensation of x_k is realized by

$$x_{c_k} = \text{ round}\left(x_k - \hat{e}(x_k, x_{k-1}) + \eta\right), \tag{4.33}$$

where η is a random number to dither the round function's quantizing errors.

4.5 Calibration Overview

With the mathematics of the multi-band DAC calibration scheme described, a step-by-step procedure can be developed.

1. Calculate the Delay Normalization with equation (3.18) providing a consistent phase reference between sent DAC samples and received ADC samples.

2. Using equation (3.19) perform the Linear Calibration so the gains and phases of the system are accounted for.

3. Find the FFT of the ADC output and select the transform components for the bins in the measurement band, either i_{aB} or i_{aL}. Then using the linear calibration gains, form the measurement vector $\vec{\mathcal{E}}_t$ found in equation (4.23) for both the bandpass and lowpass measurements.

4. Create the matrices $\tilde{\mathbf{B}}$ and $\vec{\mathbf{E}}$ introduced in equation (4.26).

5. Calculate basis function weights $\vec{w}$ from $\tilde{\mathbf{B}}$ and $\vec{\mathbf{E}}$ using the SVD technique in Section 4.3.1, taking D singular values.

6. Create and compensate a random input sequence using equation (4.33) and check performance. If correction does not seem optimal, increase D and re-calculate $\vec{w}$. Repeat until output sequence is optimal.

It is this procedure that created the results presented in Chapter 5.

CHAPTER 5

Results

A calibration and compensation scheme has been formulated to modify the DAC's input sequence to reduce harmonic error components in its output. This chapter presents a discussion of the performance of this system. Results are obtained from both a simulated setup and the actual hardware implementation of the calibration system. Finally a discussion of some calibration refinements that were made is included.

5.1 Simulated Results

Before the hardware could be tested it was necessary to test a simulated system to ensure the methods behind the wideband DAC calibration were correct. The simulation used a DAC model with second order effects dependent on the current input code and the previous input code. All other parts of the system (lowpass filter, bandpass filter, ADC, data cache ...) were also simulated to provide a good model of the actual hardware.

5.1.1 Simulation Selection of D Singular Values

To select the proper D value (Section 4.3.1) to terminate the SVD calculation, a test set of five tones was chosen to check the harmonic improvement for each value of D $(1, 2, \ldots 100)$. For this test set, a lowpass measurement band of $0 \rightarrow 6.3$ MHz and then a bandpass measurement band of $27.3 \rightarrow 34.4$ MHz were used. For each D, new basis function weights $\vec{w}$ were generated and used to compensate the test signal. The resulting SFDR for each D value was measured and is shown in Figure 5.1. Since the best performance occurred at $D = 76$, 76 singular values was used to calculate of the basis function weights.

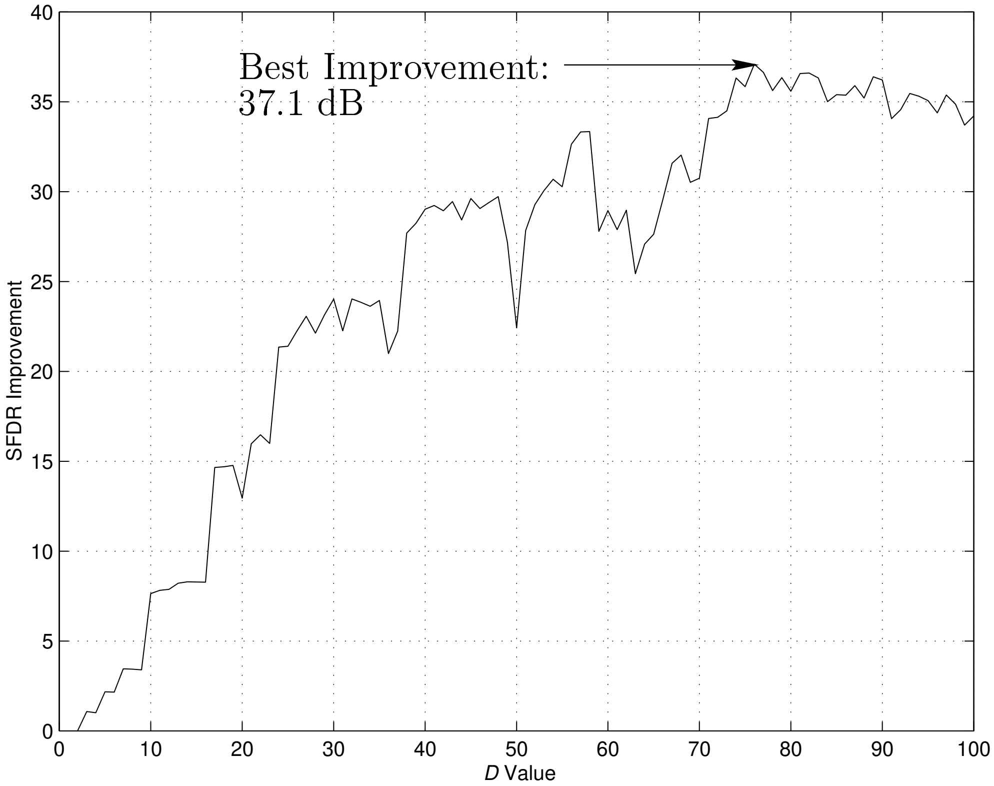

Figure 5.1: Simulated SFDR Improvement for 100 D values

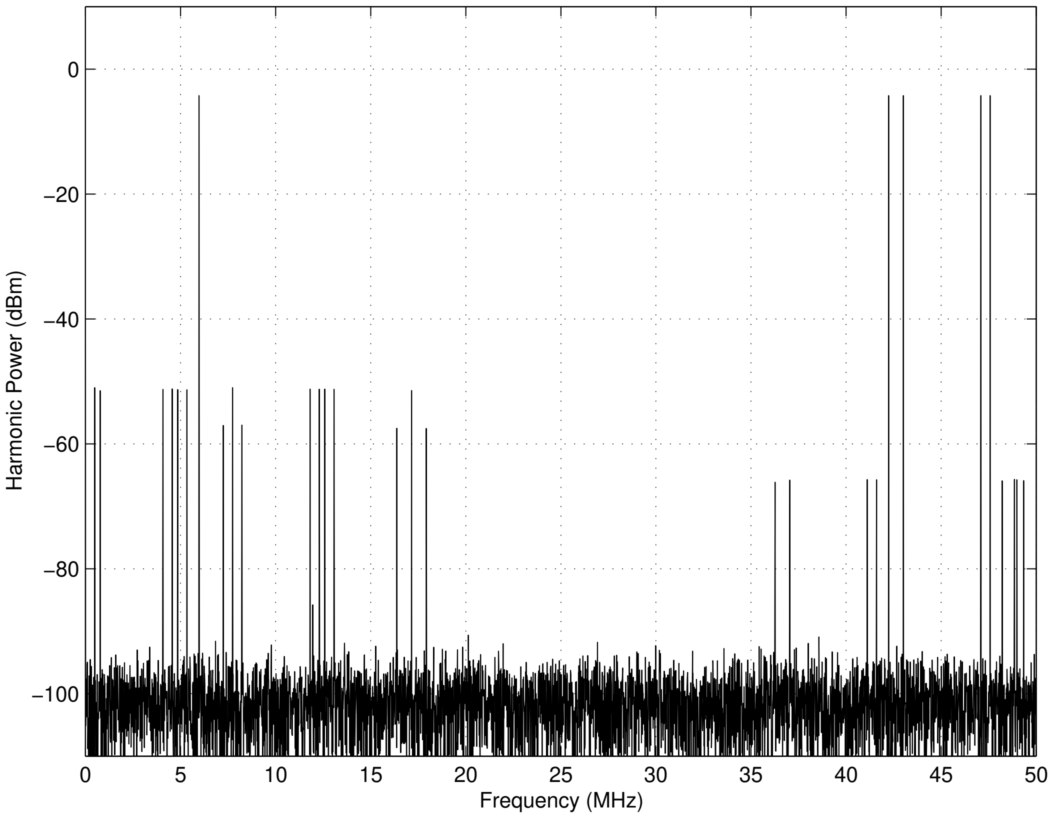

Figure 5.2: Simulated Results Showing an Uncompensated Spectrum

Figure 5.2 shows the simulated uncompensated DAC output for a five tone signal. One can see the harmonic and intermodulation distortion in this figure which should be removed by the calibration routine. Figure 5.3 shows the simulated compensated DAC output. Notice that all of the harmonics have been removed. These results give motivation to try the routine on the hardware system.

5.2 Hardware Results

The hope was to use the same code used on the simulation on the hardware to achieve similar, wideband results. The hardware setup made use of a lowpass measurement band of $0 \rightarrow 10$ MHz and then a bandpass measurement band of $27.1 \rightarrow 33.7$ MHz. Figure 5.4 shows the output spectrum of the DAC when driven

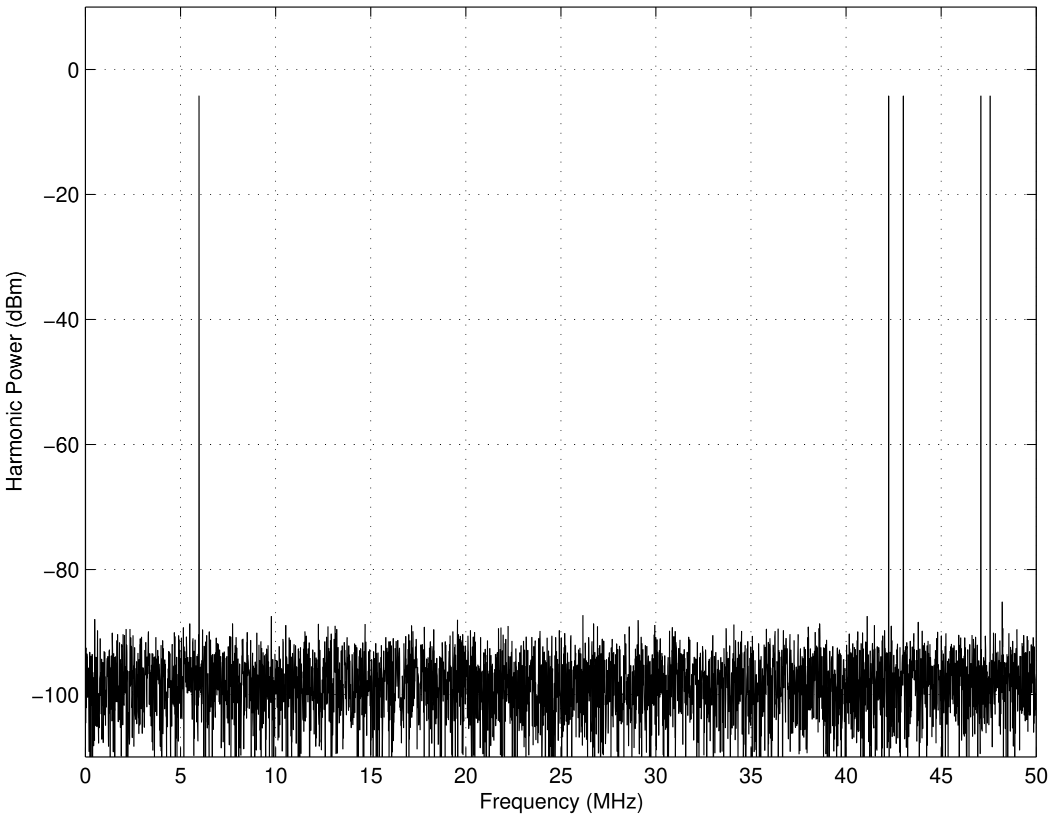

Figure 5.3: Simulated Results Showing a Compensated Spectrum

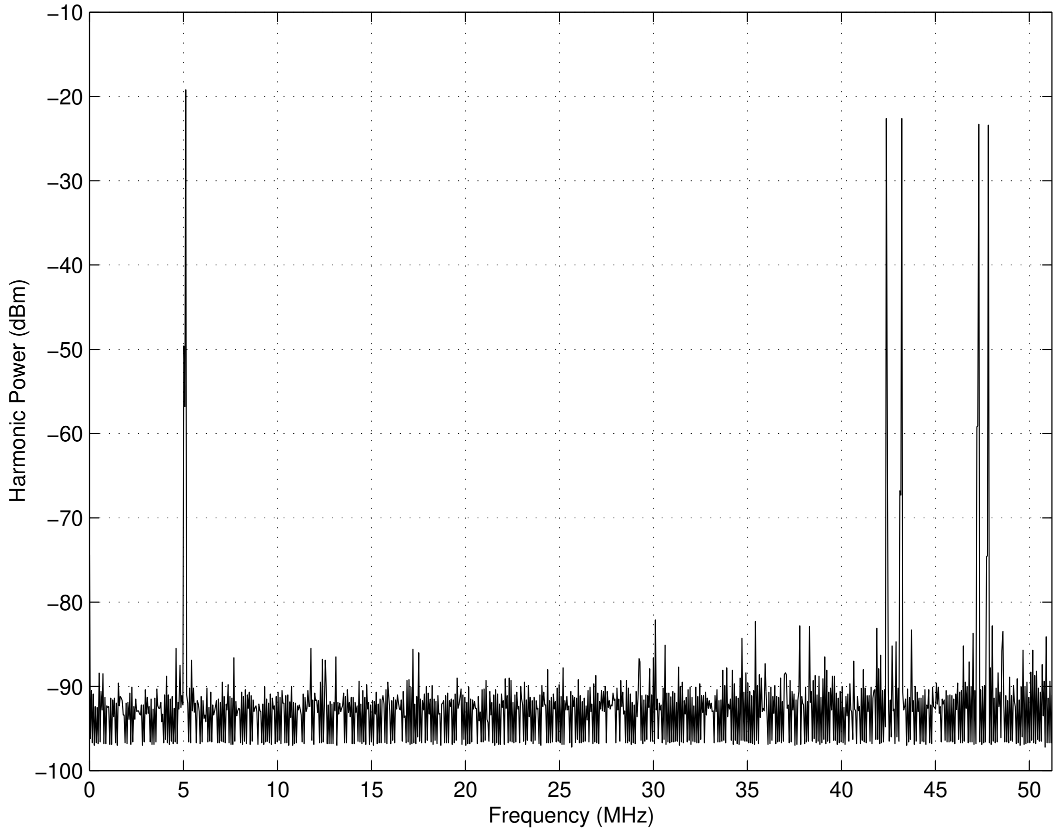

Figure 5.4: Uncompensated Output Spectrum of a 102.4 MSPS DAC

by the set of five test tones which were used to test the hardware implementation. These tones are a good choice as they produce harmonic and intermodulation distortion which lies across the whole band of the DAC output. Several tests were run. First shown is the result depicting calibrations using the exact procedure as described in Section 4.5. Unfortunately, even for the optimal D value, this was not successful as depicted in Figure 5.5 Since the higher frequencies of the spectrum were not calibrated selection of D was very difficult. Checking the SFDR was useless if the higher frequency terms were still present. Selecting D became a process of observing the DAC output spectrum for several values of D and choosing the best result. It is this unsuccessful result that led to a few calibration refinements.

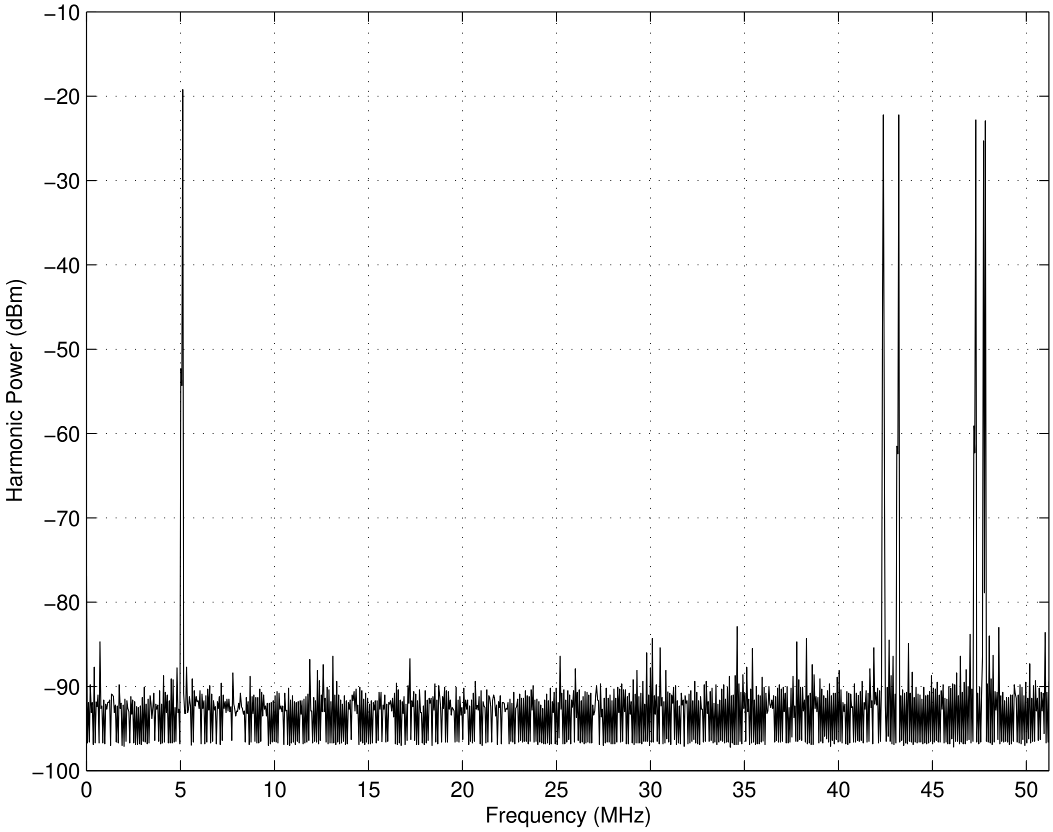

Figure 5.5: First Cut Compensated Output Spectrum of a 102.4 MSPS DAC

5.2.1 Calibration Refinements

In an attempt to correct harmonics that were unsuccessfully corrected in Figure 5.5, it was determined that the calibration signal needed to be considered further. The Riley's attempt used 100 sets of test tones of size 4096 each. This produced $100 * 4096$ input samples to cover the input space. This thesis attempted to create an error characteristic based on $2 * 8192$ (one set of 8192 samples for each the lowpass and bandpass measurement) input samples. It is this difference between the number of samples used to calculate the error characteristic that drove one focus of the calibration refinement.

Also noticed was the amount of power which the error terms were introducing. For most five tone signals, the error terms did not have power levels much above -80 dBm. Before these error terms are handed to the ADC, they are further attenuated by the filter and power splitter as shown in Figure 3.3. Upon inspection of the ADC output it was found that these error terms were only exciting at most four or five LSB's of the ADC. That represents only a very small portion of the ADC's dynamic range.

Because of these two discoveries it was determined to try the previous method of filling the input space by using several random (this thesis used as many as 50)input signals. The hope here is not only to provide more combinations of current input code - previous input code, but to place more fundamental tones in the measurement bands. This will give the error terms more range in the ADC output due to the presence of a fundamental with a power level of around -20 dB-m. Results from this attempt appear in Figure 5.6. While this did provide much better results than the original attempt, it still did not provide compensation for the highest end of the DAC output spectrum. A set of 112 basis functions. Where the first 100 were the same as found in this thesis, the last 12 were used to account for bit transition errors. This set of basis functions were used and did not provide

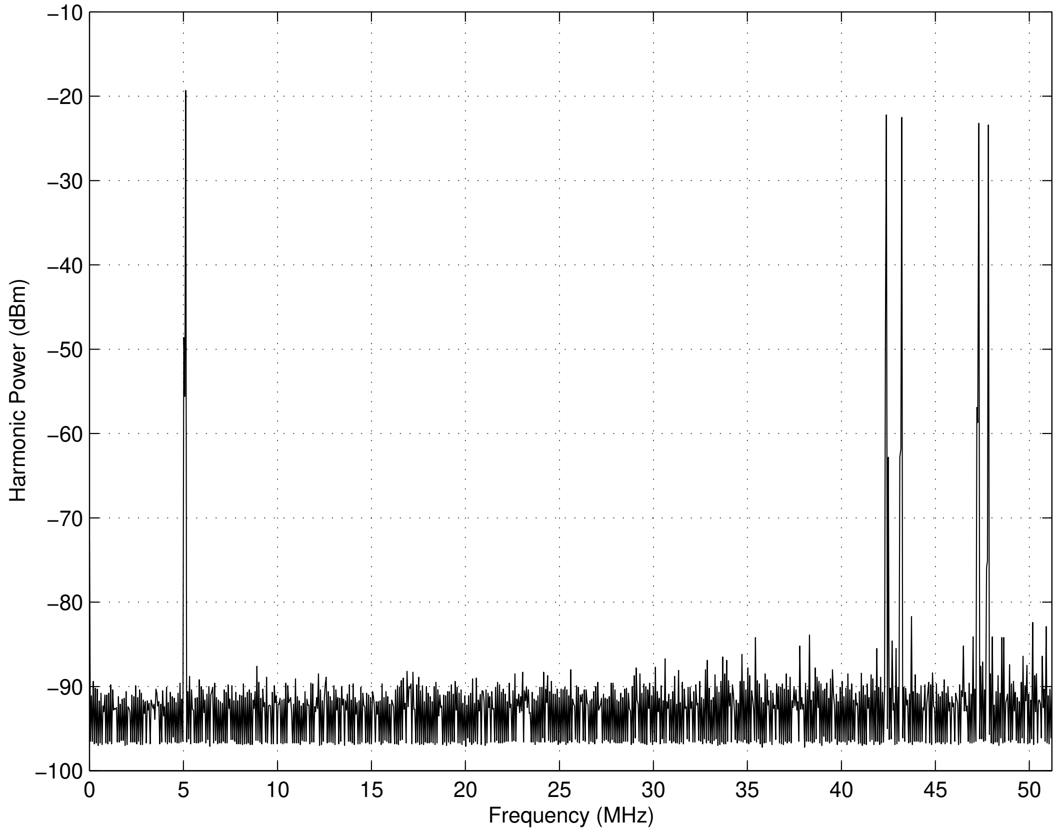

Figure 5.6: Second Cut Compensated Output Spectrum of a 102.4 MSPS DAC

any improvements. Also, the iterative search used in Riley's work to find the best input sequence was tested. This also did not provide any improvements.

To better investigate the performance of the calibration scheme a few more experiments were conducted. Of interest was the effects of the lowpass and bandpass measurements. To accomplish this, calibrations were made using only either the lowpass or bandpass measurements from the previous example. This provided a comparison between the errors being corrected by either band. Figure 5.7 shows the effects of the lowpass calibration. This illustrates which tones the lowpass calibration can effect. One can see that indeed the distortion in the lowpass measurement band is removed but distortion remains at higher frequencies. Figure 5.8 shows the effects of the bandpass calibration. Again, the distortion in the bandpass measurement band has been improved but in this case the distortion in the lower frequencies has been increased. These two results depict the difference in the error characteristic derived from the two measurement bands.

Finally, it was necessary to test another set of input frequencies to prove that the mutli-band calibration scheme does hold for multiple sets of input frequencies. A set of tones were chosen to match the tones shown in Figure 2.7 and Figure 2.8 to compare this thesis' results to earlier work [6]. The same weights that were used to create the multi-band results of Figure 5.6 were used. Figure 2.8 shows about 47 dB of SFDR. However, if the ADC clock feed-through of $f_s/4$ term is ignored the SFDR is 53 dB. Also, many harmonic terms are still present in the output. This thesis provided an SDFR of 65 with the $f_s/4$ term totally removed from the output spectrum and much of the distortion across the band removed; a dramatic improvement. This comparison shows the improvement this thesis has made in not only the quality of the DAC output but also the calibration effectiveness.

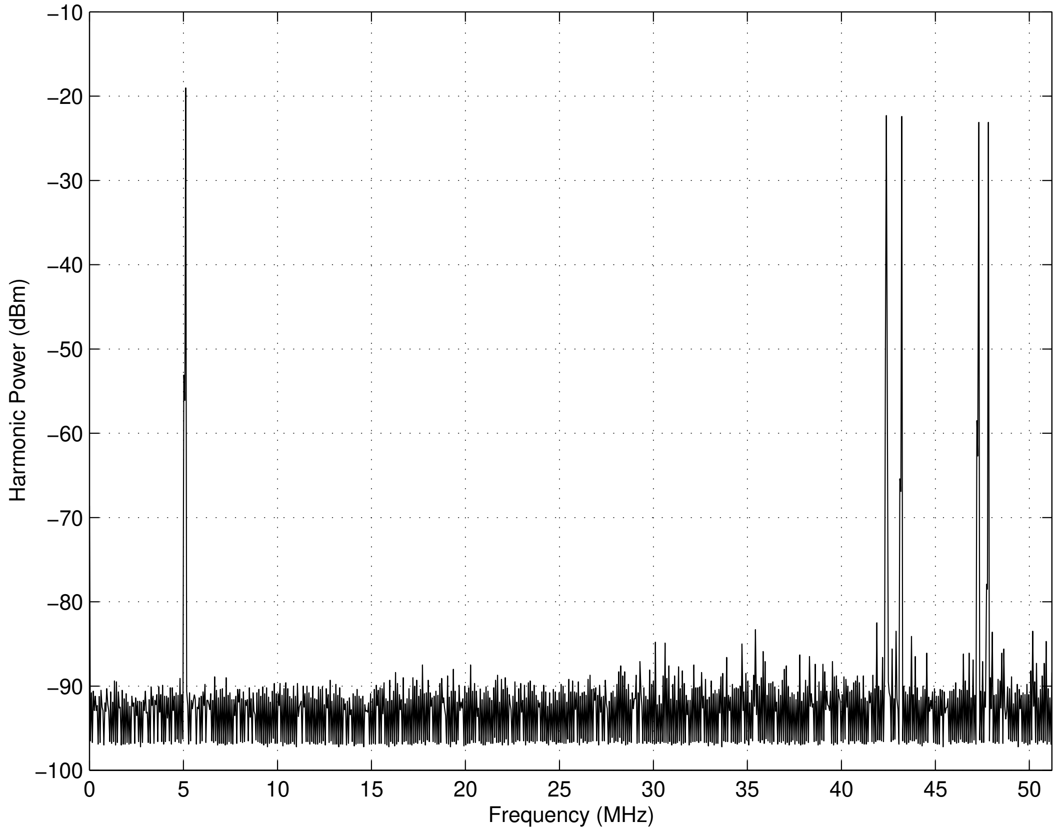

Figure 5.7: Lowpass Calibration Compensated Output Spectrum for a 102.4 MSPS DAC

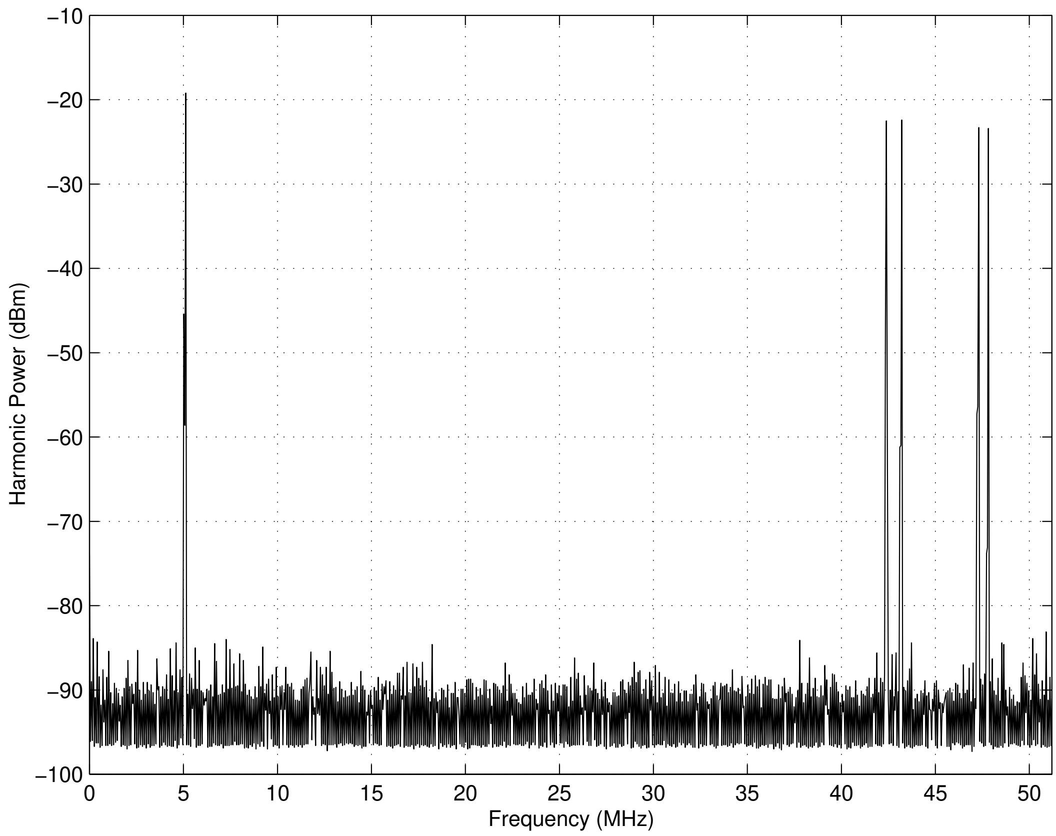

Figure 5.8: Bandpass Calibration Compensated Output Spectrum for a 102.4 M-SPS DAC

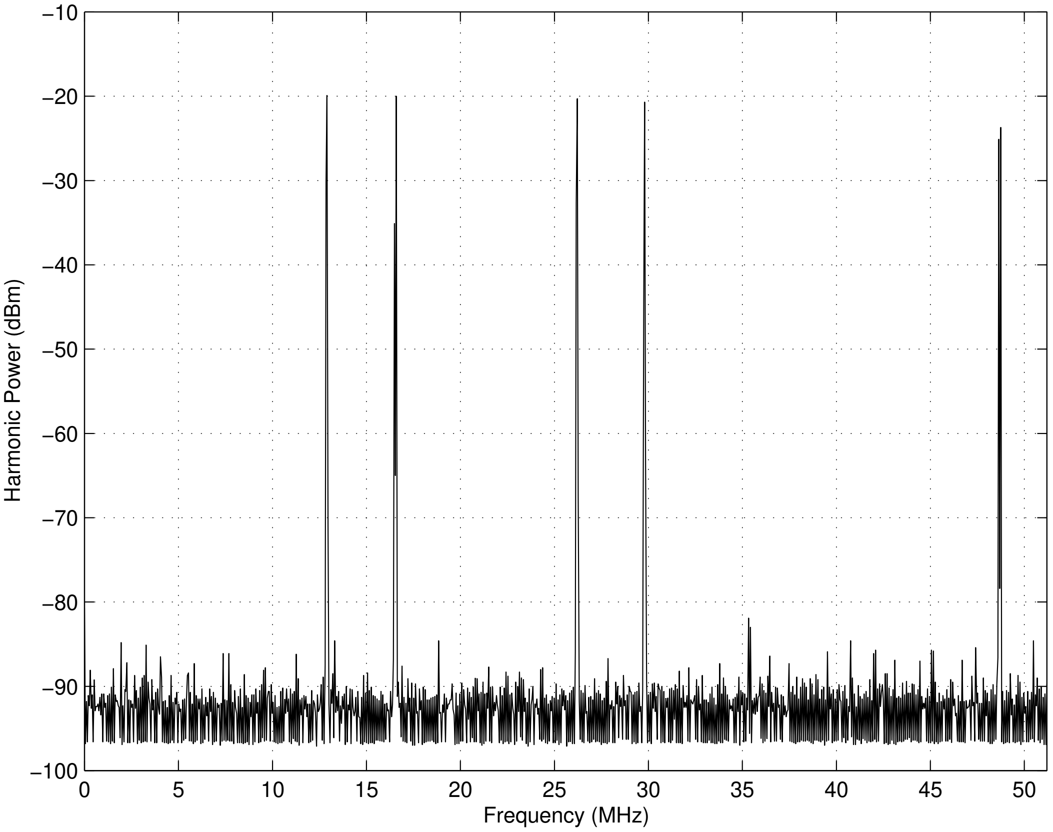

Figure 5.9: Second Example of an Uncompensated Output Spectrum for a 102.4 MSPS DAC

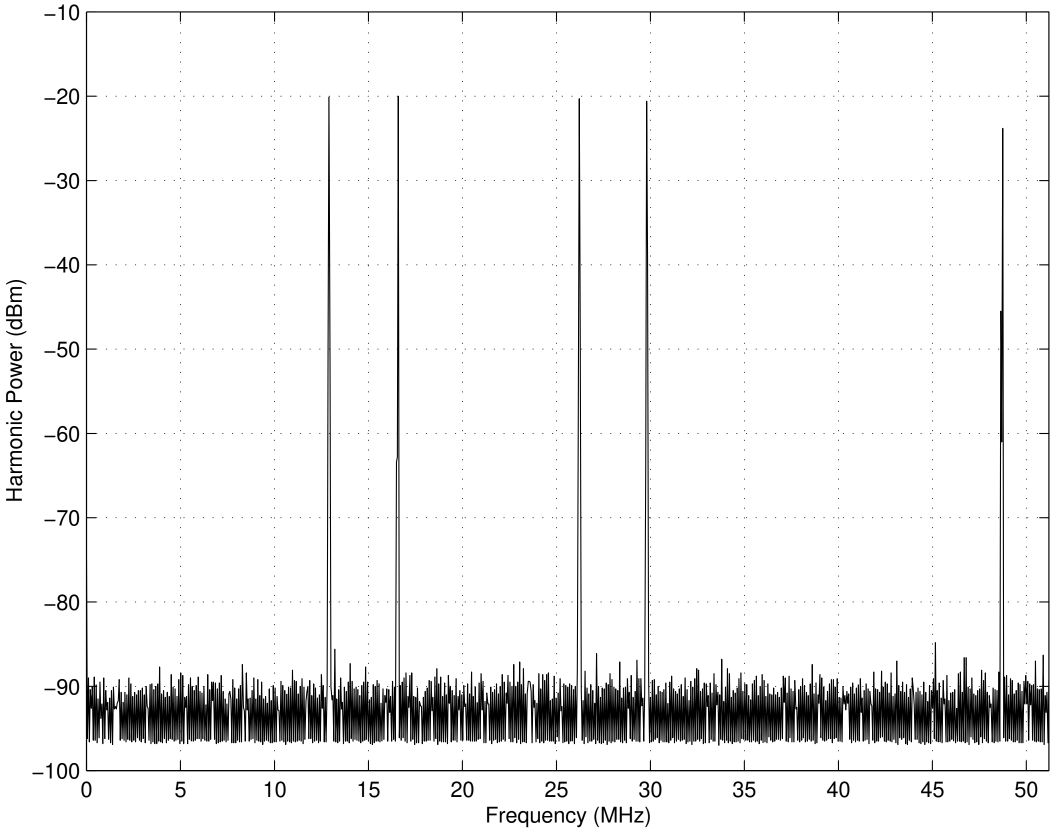

Figure 5.10: Second Example of a Compensated Output Spectrum for a 102.4 MSPS DAC

CHAPTER 6

Conclusions and Future Work

Several rewarding results were found in the development of this thesis.

1. The new DAC hardware provided immediate improvements on SFDR measurements. Whereas the the old hardware had a SFDR (for a five tone signal) of 50 dB, the new hardware achieves a SFDR of 65 dB. One improvement that lead to a large gain in SFDR was the elimination of the ADC clock feed-through into the DAC output spectrum.

2. The new DAC hardware provided the ability to reproduce experiments. The old hardware was very sensitive to any variations of anything attached to the setup or near the setup. A person standing near the old setup could improve the SFDR by 10 dB. The new hardware provides a stability that the old hardware could not.

3. Two measurement bands can be used to create an error characteristic for the DAC. This new error characteristic is capable of reducing harmonic error in both calibration bands.

4. A SVD technique can be implemented in solving for basis function weights. This is a helpful technique in solving nearly singular matrices which can produce unwanted solutions.

5. Selecting a calibration signal to cleverly fill the current input code - previous input code space can be accomplished.

6. Hardware results showing the success of the inclusion of the second band measurement are provided.

An obvious conclusion from this work can be made. It is possible to use two separate frequency bands to compensate a DAC's input sequence to reduce harmonic distortion. This is an encouraging result as the two bands did hold error information that was indeed dependent on the current input code and the previous input code. Another conclusion that can be made from the many experiments is that the lower frequency band of the DAC output was much easier to correct. The lowpass calibration almost always worked very well for bandwidths under 20 MHz.

It should be stated that DAC calibration still has much work ahead. This thesis and the previous thesis provided some good insight but there is still much to be discovered to properly produce an error model which can provide a wideband DAC calibration. Future work would include developing a system to increase the error power given to the ADC. The hardware has been improved to the point were the DAC errors are small and so measuring them becomes challenging. By amplifying the DAC output, the error would become easier to measure. Another improvement would be to increase the speed of the linear calibration. The process of sending a set of data to the DAC is a very slow procedure. In this thesis to generate the linear characterization $\vec{G}$, there were as many as 810 bins in one calibration band. This would require 810 individual sinusoids to be sent to the DAC, a painstakingly long process. Also, once the hardware tests began, the selection of D almost became impossible. Certainly there were some values that provided better results, but a good selection method was not achieved. A closer inspection of basis function type and how they are centered could also be given some thought. A final improvement would be compensation of the entire output band of the DAC. For this to be accomplished another error mechanism needs to be identified to compensate these terms.

References

[1] Analog Devices. *12-bit, 41 MSPS Monolithic A/D Converter*, 1996. REV. A.

[2] Paul Hendriks. Specifying communication DACs. *IEEE Spectrum*, pages 58–69, July 1997.

[3] Donald M. Hummels and Fred H. Irons. Sampling systems - analog to digital converter design and applications. Technical report, University of Maine, Orono, September 1996.

[4] Dr. James Murphy. “Digital Receiver Technology Program”. Technical report, *(web-ext2.darpa.mil/ETO/ADC/)*, Defense Advanced Research Program Agency, November 1998.

[5] Alan V. Oppenheim and Ronald W. Schafer. *Discrete-Time Signal Processing.* Prentice Hall, 1989.

[6] K. Riley. Dymanic compensation of digital to analog converters. Master's thesis, University of Maine, Dept. of Electrical and Computer Eng., Orono Maine, August 1998.

[7] L.L. Scharf. *Statistical Signal Processing: Detection, Estimation, and Time Series Analysis.* Addison-Wesley, Reading, Massachusetts, 1991.

Biography of the Author

Ryan Cornelis Jacobson was born in Portland, Maine on May 4, 1975. He completed his high school education from Winthrop High School in Winthrop, Maine in 1993.

He entered the University of Maine in the fall of 1993 and obtained his Bachelor of Science degree in Electrical Engineering in 1997.

In May 1997, he was enrolled for graduate study in Electrical Engineering at the University of Maine and served as a Research Assistant. His current research interests include data conversation and signal processing. He is a member of Tau Beta Pi and Eta Kappa Nu, and his interests include golf, tennis, basksetball, and travelling. He is a candidate for the Master of Science degree in Electrical Engineering from the University of Maine in August 1999.