ECE 471 – Embedded Systems
Lecture 3

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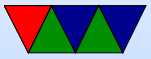
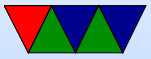
Announcements

- HW#1 will be given out on Thursday
- Read Chapter 2 in Textbook

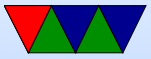


Computer Architecture Hierarchy

GUI programming	android programmin
system libraries compilers	embedded systems/com
operating system/device-drivers raw metal/asm language	embedded systems
cpu/memory	comp architecture
functional unit	comp architecture / V
gates/transistors	VLSI
process level (silicon)	VLSI

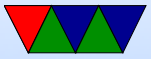


The ARM Architecture



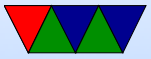
Brief ARM History

- **A**corn **R**ISC **M**achine. Acorn was a computer company in the UK in the 1980s
- Wanted a chip to succeed 6502. Decided to make one themselves. (Good idea, 65816 a pain and only 16-bit)
- 6502 was the chip in Commodore 64, Apple II, NES, Atari 2600
- Fun fact: 6502 co-designed by UMaine alum Chuck Peddle



ARM Business Plan

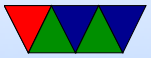
- IP Licensing company. Does not fab own chips. License to other companies
- Other companies take the design, put on SoC, attach whatever other logic blocks are needed
- Relatively small company compared to Intel which not only deigns the chip, but fabs, etc.



AMBA Bus Protocol

Advanced Microcontroller Bus Architecture

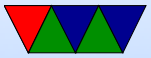
- ARM System Bus (ASB), ARM Peripheral Bus (APB)
- ARM High Performance Bus (AHB)
- Common bus, various companies can provide logic blocks for it, can swap in and out ARM cores as needed.



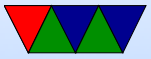
Models – Confusing

Architecture vs Family

- ARMv1 : ARM1
- ARMv2 : ARM2, ARM3 (26-bit, status in PC register)
- ARMv3 : ARM6, ARM7
- ARMv4 : StrongARM, ARM7TDMI, ARM9TDMI
- ARMv5 : ARM7EJ, ARM9E, ARM10E, XScale



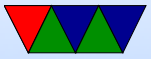
- ARMv6 : ARM11, ARM Cortex-M0 (Raspberry Pi)
- ARMv7 : Cortex A8, A9 ,Cortex-M3 (iPad, iPhone, Pandaboard, Beagleboard, Beaglebone)
- ARMv8 : Cortex A-50 (64-bit)



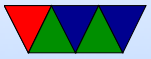
Various abbreviations in Model Names

For example, ARM7DTMI

- "Application" ARM Cortex-A
- "Real-time" ARM Cortex-R
- "Micro-controller" ARM Cortex-M
- "E" means DSP instructions
- "M" improved multiplier

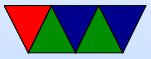


- “T” THUMB
- “J” Jazelle (java bytecodes)
- D/I Debug/ICE
- EE – ThumbExecutionEnvironment, Just-in-time
- NEON – SIMD
- VFP – Floating point

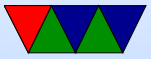


Cortex A9

- Pandaboard, iPad2, etc
- Multi-core (1-4 cores)
- L1 cache 32kB i/d
- configurable L2 cache
- out-of-order super-scalar
- neon SIMD

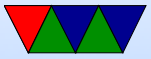


- VFP3 floating point (optional)
- Up to 2GHz.



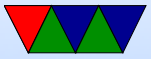
STM32F4

- Used in Hummels Class
- ARM Cortex-M4F core, 180 MHz. F is for Floating point
- Static RAM, 64K core coupled memory (CCM), 4K battery-backed, 80B tamper-detect erase.
- Flash ROM: 512 - 2048 KB general purpose, 30 KB system boot
- Lots of busses: USB, CAN, SPI, I^2S, I^2C, UART, SDIO

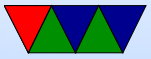


for SD/MMC, ADCs, DACs, GPIOs, DMA, RTC, CRC engine, RNG

- Some packages support external memory bus
- Instruction set: Thumb, Thumb-2, Saturating Math, DSP, FPU
- ARMv7E-M architecture
- 1-cycle 32-bit hardware multiply, 2-12 cycle 32-bit hardware divide, saturated math support

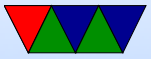


- DSP extension: Single cycle 16/32-bit MAC, single cycle dual 16-bit MAC, 8/16-bit SIMD arithmetic.
- Floating-Point extension (silicon option): Single-precision floating point unit, IEEE-754 compliant.
- 3-stage pipeline with branch speculation
- optional 8 region memory protection unit (MPU)



Cortex-M0

- Small core, optimized for small die size (cheaper!)
- ARMv6-M architecture[6]
- Thumb (most), missing CBZ, CBNZ, IT (predication)
- Thumb-2 (subset), only BL, DMB, DSB, ISB, MRS, MSR.
- 32-bit hardware multiply, 1-cycle or 32-cycles (silicon option)



- 3-stage pipeline (in-order)