ECE 471 – Embedded Systems Lecture 2

Vince Weaver

`http://www.eece.maine.edu/~vweaver`

`vincent.weaver@maine.edu`

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Announcements

- HW#1 will be posted today, due next Thursday.
  I will send out an e-mail when HW posted.
  Be sure you are checking the e-mail you have as your primary in mainestreet.
  Homeworks are typically submitted by e-mail, and I will reply with the grade.

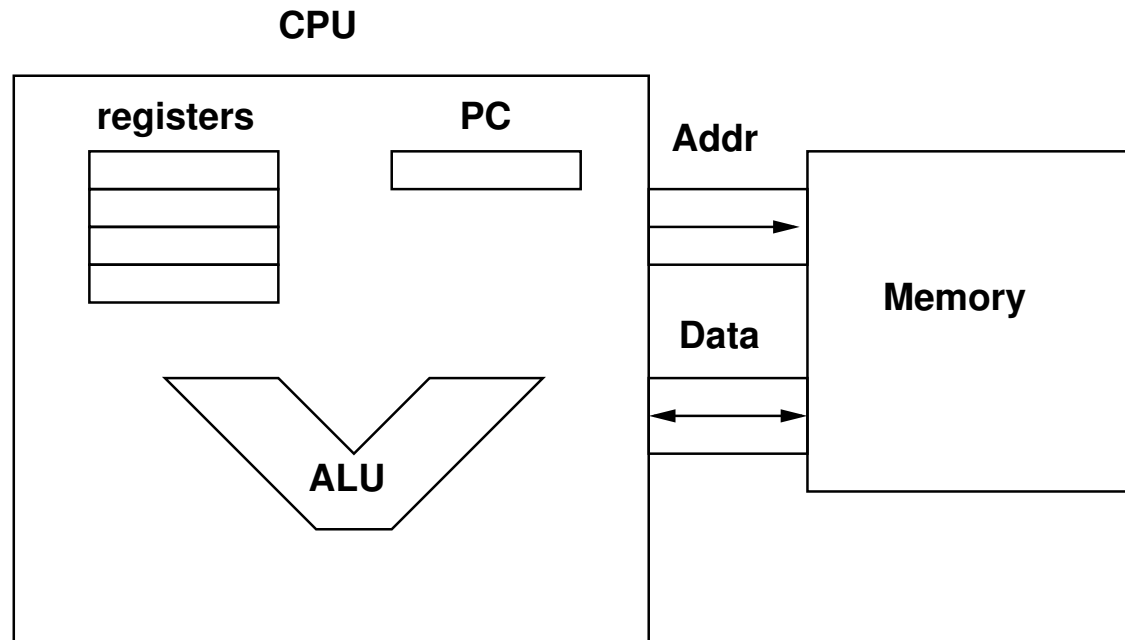- The class notes are posted to the website.

Microprocessors

- First one considered to be 4004 by Intel (for use in calculator)

- First to include all of a CPU on one chip. Before that there were processors, but often were made out of many discrete chips (sometimes entire boards full of logic)

8-bit vs 16-bit vs 32-bit

CPU

registers **PC** **Addr**

Memory

Data

ALU

- What makes a processor 8-bit vs 16-bit vs 32-bit?
  - The size of the registers?
  - The size of the address bus?

- The size of the data bus?
- The size of the ALU (integer math unit)?
- The size of the PC (program counter)?
- On modern systems it typically is the integer registers, as well as the maximum size of a memory pointer (which typically is the same as the integer register size)
- On many systems though it is not as clear cut.
- A "pure" 8-bit system would have 8-bit registers (0-255), 8-bit ALU, and an 8-bit data bus. However an 8-bit address bus (only 256 bytes of RAM) is too limiting so most 8-bit processors (6502, z80, 8080, etc) had 16-

bit address busses, 16-bit PCs, and often 16-bit register capability

- Most 16-bit processors were equally complex. The 8086 had 16-bit registers and 16-bit data bus, but a 20-bit address bus with complex addressing. To complicated things, the 8088 was 8086 compatible but had only an 8-bit data bus (to save cost, with the side effect of making memory accesses take twice as long)
- Most 32-bit processors have 32-bit registers and 32-bits of address space, but that limits to 4GB so some have extensions (x86 and ARM) allowing 36-bits of address

space. And data bus has been made complex by caches and are often quite large. And often there are larger registers on chip (64-bit or 80-bit floating point, 128-bit SSE, 256-bit AVX)

- Most 64-bit processors have 64-bit registers, but their address bus is often limited (to 36 - 40 bits, sometimes 48-bits, this is complicated by virtual memory)
- Do machines have to be a power-of-two in bitness? No, not necessarily. 36-bit machines were once quite popular.

Example Embedded Platforms

- 8051 microcontroller from intel, 8-bit
  8 8-bit registers (one special 16-bit), 8-bit ALU
  8-bit data bus, 16-bit address bus (64kB)
  bank-selectable register set
  interrupts, timers
  128 Bytes on-chip RAM
  4k on-chip ROM
  special boolean engine

- 68HC12 microcontroller

- ARM Cortex-M0 in the STM32L. See later.

- Other common embedded systems you might have heard of: PIC – generally 8 or 16bit but complicated (instructions can be 12 or 14)
ARDUINO – various AVR 8/16/32-bit micro controllers AVR

The ARM Architecture

Brief ARM History

- **A**corn **R**ISC **M**achine. Acorn was a computer company in the UK in the 1980s

- Wanted a chip to succeed 6502. Decided to make one themselves. (Good idea, 65816 a pain and only 16-bit)

- 6502 was the chip in Commodore 64, Apple II, NES, Atari 2600

- Fun fact: 6502 co-designed by UMaine alum Chuck Peddle

RISC aside

- Simple decode. Load/store. Fixed instruction width. 3-operand.

- MIPS

- ARM (predication, auto-increment, barrel shifter)

- x86 (crazy)

ARM Business Plan

- IP Licensing company. Does not fab own chips. License to other companies

- Other companies take the design, put on SoC, attach whatever other logic blocks are needed

- Relatively small company compared to Intel which not only deigns the chip, but fabs, etc.

AMBA Bus Protocol

Advanced Microcontroller Bus Architecture

- ARM System Bus (ASB), ARM Peripheral Bus (APB)

- ARM High Performance Bus (AHB)

- Common bus, various companies can provide logic blocks for it, can swap in and out ARM cores as needed.

Models – Confusing

Architecture vs Family

- ARMv1 : ARM1
- ARMv2 : ARM2, ARM3 (26-bit, status in PC register)
- ARMv3 : ARM6, ARM7
- ARMv4 : StrongARM, ARM7TDMI, ARM9TDMI
- ARMv5 : ARM7EJ, ARM9E, ARM10E, XScale
- ARMv6 : ARM11, ARM Cortex-M0 (Raspberry Pi A/B)
- ARMv7 : Cortex A8, A9, A15, A7, Cortex-M3 (iPad, iPhone, Pandaboard, Beagleboard, Beaglebone, Pi2)

- ARMv8 : Cortex A50, A57 (64-bit)

Various abbreviations in Model Names

- Modern Cortex Processors
  - "Application" ARM Cortex-A
  - "Real-time" ARM Cortex-R
  - "Micro-controller" ARM Cortex-M
- ARM7 Processors (example armv4 ARM7TDMI)
  - "E" means DSP instructions
  - "M" improved multiplier
  - "T" THUMB
  - "J" Jazelle (java bytecodes)

- ○ "D" Debug
- ○ "I" ICE (In-circuit Emulator)
- ○ "EE" ThumbExecutionEnvironment, Just-in-time
- ○ NEON – SIMD
- ARM11 Processors (Raspberry Pi is armv6 BCM2835 ARM1176JZF-S)
  - ○ (All have Thumb)
  - ○ S – Synthesizable
  - ○ J – Java Extension
  - ○ Z – TrustZone
  - ○ F – Vector Floating Point Coprocessor

Cortex A9

- Pandaboard, iPad2, etc
- Up to 2GHz.
- Multi-core (1-4 cores)
- Also on-board Cortex-M codec decoders
- L1 cache 32kB i/d
- configurable L2 cache
- out-of-order super-scalar
- neon SIMD
- VFP3 floating point (optional)

STM32L-Discovery

- Used in 271
- ARM Cortex M3 core, 128kB flash, 16kRAM
- ADC, DAC
- Low-power consumption
- i2c, spi, usart
- LCD display
- USB
- Timers
- Thumb2

STM32F4

- Used in Hummels Class
- ARM Cortex-M4F core, 180 MHz. F is for Floating point
- Static RAM, 64K core coupled memory (CCM), 4K battery-backed, 80B tamper-detect erase.
- Flash ROM: 512 - 2048 KB general purpose, 30 KB system boot
- Lots of busses: USB, CAN, SPI, I^2S, I^2C, UART, SDIO for SD/MMC, ADCs, DACs, GPIOs, DMA, RTC, CRC engine, RNG

- Some packages support external memory bus
- Instruction set: Thumb, Thumb-2, Saturating Math, DSP, FPU
- ARMv7E-M architecture
- 1-cycle 32-bit hardware multiply, 2-12 cycle 32-bit hardware divide, saturated math support
- DSP extension: Single cycle 16/32-bit MAC, single cycle dual 16-bit MAC, 8/16-bit SIMD arithmetic.
- Floating-Point extension (silicon option): Single-precision floating point unit, IEEE-754 compliant.
- 3-stage pipeline with branch speculation

- optional 8 region memory protection unit (MPU)

Cortex-M0

- Small core, optimized for small die size (cheaper!)
- ARMv6-M architecture[6]
- Thumb (most), missing CBZ, CBNZ, IT (predication)
- Thumb-2 (subset), only BL, DMB, DSB, ISB, MRS, MSR.
- 32-bit hardware multiply, 1-cycle or 32-cycles (silicon option)
- 3-stage pipeline (in-order)

Other Crazyness

- BIG.little