ECE571: Advanced Microprocessor Design – Homework 6 Prefetching Fall 2024

Due: Friday 25 October 2024, 5:00pm

Create a document that contains the data and answers described in the sections below. A .pdf or .txt file is preferred but I can accept MS Office or Libreoffice format if necessary.

1. Bzip2 prefetch behavior on the x86 Haswell-EP Machine

For this section, log into the Haswell-EP machine just like in previous homeworks.

Run the bzip2 benchmark on the Haswell machine.

(a) Measure (in one command) bzip using the following events: 12_rqsts.all_demand_references which is total L2 cache accesses, 12_rqsts.demand_data_rd_miss which is total demand L2 cache misses, and 12_rqsts.all_pf which is total prefetches into the L2 cache.

```
perf stat -e l2_rqsts.all_demand_references:u,\
l2_rqsts.demand_data_rd_miss:u,\
l2_rqsts.all_pf:u \
/opt/ece571/401.bzip2/bzip2 -k -f ./input.source
```

Note, if the program finishes instantly with an error message, be sure you have input.source in your current directory. You can recopy it with

cp /opt/ece571/401.bzip2/input.source .

Calculate the L2 cache miss rate from the first two results (misses/total), the third event is just informational, it in theory tracks total number of prefetches. Note all 3 values, the rate, and total time.

2. Software Prefetching and bzip2 on Haswell-EP

(a) Re-run the previous prefetch results on Haswell, but instead of running bzip2 run bzip2.swprefetch which was compiled with -fprefetch-loop-arrays which enables sw prefetch instructions.

Record the miss rate and total time.

```
perf stat -e l2_rqsts.all_demand_references:u,\
l2_rqsts.demand_data_rd_miss:u,\
l2_rqsts.all_pf:u \
/opt/ece571/401.bzip2/bzip2.swprefetch -k -f ./input.source
```

3. equake_l prefetch behavior on the x86 Haswell-EP Machine

Run equake_l:

```
(a) perf stat -e l2_rqsts.all_demand_references:u,\
    l2_rqsts.demand_data_rd_miss:u,\
    l2_rqsts.all_pf:u \
    /opt/ece571/equake_l.specomp/equake_l < \
    /opt/ece571/equake_l.specomp/inp.in</pre>
```

Calculate the L2 cache miss rate from the first two results, also note the total time.

4. equake_l software prefetch behavior on the x86 Haswell-EP Machine

Run equake_l with software prefetch enabled:

```
(a) perf stat -e l2_rqsts.all_demand_references:u, \
    l2_rqsts.demand_data_rd_miss:u, \
    l2_rqsts.all_pf:u \
    /opt/ece571/equake_l.specomp/equake_l.swprefetch < \
    /opt/ece571/equake_l.specomp/inp.in</pre>
```

Calculate the L2 cache miss rate from the first two results, also note the total time.

5. Hardware Prefetch Disabled

It is possible to disable hardware prefetch on modern Intel processors. See:

https://software.intel.com/en-us/articles/disclosure-of-hw-prefetcher-control-on-some-intel-processors
for details.

It requires root permissions, so I have re-run the four experiments above with the results summarized in the table below.

benchmark	L2-total	L2-miss	L2-prefetches	time
bzip2	295,148,679	130,346,668	62,885	4.00
bzip2.swprefetch	295,348,496	131,765,612	59,583	4.00
equake_1	29,939,302,233	20,929,001,917	9,241,889	62.94
equake_l.swprefetch	29,829,058,607	20,921,333,239	9,168,505	59.29

Haswell-EP L2 cache results, HW Prefetch Disabled

6. Short Answer Questions

- (a) Did enabling software prefetch help on bzip2? (i.e. compare the results in question 1 and question 2?)
- (b) Did enabling software prefetch help on equake_1? (i.e. compare the results in question 3 and question 4?)
- (c) How did turning off the prefetcher affect the bzip2 results (i.e. question 1 vs question 5?)
- (d) How did turning off the prefetcher affect the equake_l results (i.e. question 3 vs question 5?)
- (e) With the hardware prefetcher disabled, did enabling software prefetch help at all? (question 5)
- (f) Why do you think the software prefetch performance is so underwhelming?

7. Submitting your work.

- Create the document containing the data as well as answers to the questions asked.
- Please make sure your name appears in the document.
- e-mail the file to me by the homework deadline.