**ECE571: Advanced Microprocessor Design – Homework 4**

**Due: Friday 7 November 2014, 3:30PM**

Create a document that contains the data and answers described in the sections below. A .pdf or .txt file is preferred but I can accept MS Office or Libreoffice format if necessary.

1. **Bzip2 cache behavior on the x86 Haswell Machine**

   For this section, log into the Haswell machine just like in previous homeworks.

   Run the bzip2 benchmark on the Haswell machine. Recall that a bzip2 command line looks something like this:

   ```
   perf stat -e instructions:u,branches:u,r5301c4:u
   /opt/ece571/401.bzip2/bzip2 -k -f ./input.source
   ```

   (a) Measure and report the L1 instruction cache miss rate.
   Use `instructions:u` and `L1-icache-load-misses:u` for the events.

   (b) Measure and report the L1 data cache load miss rate.
   Use `L1-dcache-loads:u` and `L1-dcache-load-misses:u`

   (c) Measure and report the L1 data cache store miss rate.
   Use `L1-dcache-stores:u` and `L1-dcache-store-misses:u`

   (d) Measure and report the L3 cache miss rate
   Use `cache-references:u` and `cache-misses:u`

   (e) Measure and report the iTLB miss rate
   Use `iTLB-loads:u` and iTLB-load-misses:u

   (f) Measure and report the dTLB-load miss rate
   Use `L1-dcache-loads:u` and dTLB-load-misses:u

   (g) Measure and report the dTLB-store miss rate
   Use `L1-dcache-stores:u` and dTLB-store-misses:u

2. **Bzip2 cache behavior on the Trimslice**

   Now run the bzip2 benchmark on the Trimslice machine.

   (a) Measure and report the L1 instruction cache miss rate.
   Use `instructions` and `L1-icache-load-misses` for the events.

   (b) Measure and report the L1 data cache load miss rate.
   Use `L1-dcache-loads` and `L1-dcache-load-misses`

   (c) Measure and report the L1 data cache store miss rate.
   Use `L1-dcache-stores` and `L1-dcache-store-misses`

   (d) Measure and report the L2 cache miss rate
   Use `cache-references` and `cache-misses`

   (e) Measure and report the iTLB miss rate
   Use `instructions` and iTLB-load-misses

(f) Measure and report the dTLB-load miss rate
Use `L1-dcache-loads` and dTLB-load-misses

(g) Measure and report the dTLB-store miss rate
Use `L1-dcache-stores` and dTLB-store-misses

3. **equake_l cache behavior on the x86 Haswell Machine**

Recall that running equake looks something like this:

```
perf stat -e instructions:u,branches:u,r5301c4:u
/opt/ece571/equake_l.specomp/equake_l <
/opt/ece571/equake_l.specomp/inp.in
```

(a) Measure and report the L1 instruction cache miss rate.
Use `instructions:u` and `L1-icache-load-misses:u` for the events.

(b) Measure and report the L1 data cache load miss rate.
Use `L1-dcache-loads:u` and `L1-dcache-load-misses:u`

(c) Measure and report the L1 data cache store miss rate.
Use `L1-dcache-stores:u` and `L1-dcache-store-misses:u`

(d) Measure and report the L3 cache miss rate
Use `cache-references:u` and `cache-misses:u`

(e) Measure and report the iTLB miss rate
Use `iTLB-loads:u` and iTLB-load-misses:u

(f) Measure and report the dTLB-load miss rate
Use `L1-dcache-loads:u` and dTLB-load-misses:u

(g) Measure and report the dTLB-store miss rate
Use `L1-dcache-stores:u` and dTLB-store-misses:u

4. **Software Prefetching and bzip2 on Haswell**

(a) Re-run the L1-dcache-load cache results for bzip2 on Haswell, but instead of running `bzip2` run `bzip2.swprefetch` which was compiled with `-fprefetch-loop-arrays` which enabled sw prefetch. Record the miss rate.

(b) Do the same for `equake` by running `equake_l.swprefetch`

5. **perf mem**

Recent Haswell chips have memory access latency and type info available with PEBS.

(a) Run bzip2 one last time, but use:
`perf mem record` as the command preceding bzip2.

(b) Now run `perf mem report`

(c) Make note of the top 5 loads causing overhead

6. **Short Answer Questions**

(a) How do the various cache miss rates for bzip2 compare between the Haswell and the Trimslice?

(b) How do the various cache miss rates on the Haswell machine compare between the bzip2 and equake benchmarks?

(c) For the L1-icache-misses event, the Linux kernel uses `ICACHE:MISSES` while PAPI uses `L2_TRANS:CODE_RD` Look at the intel vol3b developer manual: `http://www.intel.com/content/www/us/en/architecture-and-technology/64-ia-32-architectures-software-developer-vol-3b-part-2-manual.html` See table 19-3 (Haswell is "4th-generation"). Look at the descriptions for these two events. Do these match the behavior you'd expect with L1-icache-misses? Do you think you get the same results using these two events?

(d) Compare the miss rate of bzip2 on Haswell when software prefetch is enabled and disabled. Does one behave better than the other? Do the same comparison for equake with and without. Does one behave better? If this is different than the bzip2 result, explain why it might differ.

7. Submitting your work.

- Create the document containing the data as well as answers to the questions asked.
- Please make sure your name appears in the document.
- e-mail the file to me by the homework deadline.