ECE 571 – Advanced Microprocessor-Based Design Lecture 16

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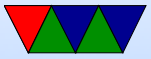
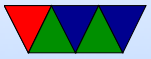
Announcements

- Project topics
- HW#8 will be similar, about a modern ARM chip



Busses

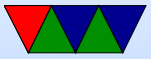
- Grey Code, only one bit change when incrementing. Lower energy on busses? (Su and Despain, ISLPED 1995).



Reading of the Webpage

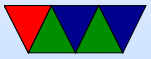
`http://anandtech.com/show/9582/intel-skylake-mo`

The Intel Skylake Mobile and Desktop Launch, with Architecture Analysis by Ian Cutress

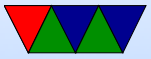


Background on where info comes from

Intel Developer Forum This one was in August



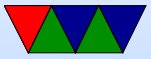
Name	tech		Year
Conroe/Merom	65nm	Tock	2006
Penryn	45nm	Tick	2007
Nehalem	45nm	Tock	2008
Westmere	32nm	Tick	2010
Sandy Bridge	32nm	Tock	2011
Ivy Bridge	22nm	Tick	2012
Haswell	22nm	Tock	2013
Broadwell	14nm	Tick	2014
Skylake	14nm	Tock	2015
Kaby Lake?	14nm	Tock	2016



Clock: tick-tock. Upgrade the process technology, then revamp the uarch.

14nm technology? Finfets? What technology are Pis at? 40nm?

14nm yields getting better. hard to get, even with electron beam lithography plasma damage to low-k silicon only 0.111nm finfet. Intel has plants Arizona, etc. Delay to 10nm 7nm? EUV?



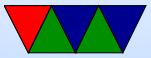
Skylake Processor – Page 1

- 4.5W ultra-mobile to 65W desktop They release desktop first these days. For example just today releasing "Xeon E5-2600 v4" AKA Broadwell-EP

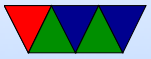
  Confusing naming i3, i5, i7, Xeon, Pentium, m3, m5, m7, etc.

  Number of pins important. Low-power stuck with LPDDR3/DDR3L instead of DDR4 possibly due to lack of pins?

  eDRAM?

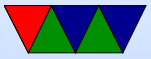


Intel no longer releasing info on how many transistors/transistor size?

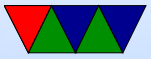


Skylake Processor – Page 2

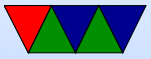
- "mobile first" design. Easier to scale up than down?
- Want to use in tablets. What % of market does intel have on tablets?
- Up to 60% lower active power (win8.1 video playback, i7-6920HQ vs i7-4910MQ)
- Up to 60% faster estimated SPECint 2006 (i5-6300HQ vs i5-4300M)



- Up to 40% better graphics On 3DMARK Sky Diver overall (m76Y75 vs m5Y71)
- Overtook AMD performance on integrated graphics (though costing more)
- Power features:
  - Fine grain power gating (core, system agent, graphics, chipset)
  - Digital PLL
  - HW and Cdyn reduction(?) (cdyn is capictance)
  - Lower Vmin

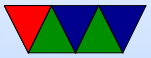


- DDR, Serial I/O power optimization
- Speed shift
- C9 display with Self Refresh Panel
- "modern standby"
- Configurable power management (i.e. the OEMs can customize, it's off chip again)



Skylake Processor – Page 3

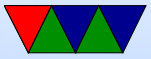
- Microacrhcitcute
- Sound DSP, faster DDR memory, advanced integrated graphics, wider core, enhanced LLC
- DDR3L and DDR4
- 16 PCIe lanes (what is PCI typically used for? external GPUs and disk)
- DMI 3.0 (8.0GT/s, 3.93GB/s), but motherboard traces



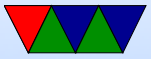
down to 7in from 8in?
DMI=direct media interface, connection between north and south bridge multiple lanes, differential signalling

- Chipset on package, low power I/O OPIO (on-package I/O) 1pJ/bit

- Haswell/Broadwell had FIVR (fully integrated voltage regulator)
  simpler design, higher temperatures, made overclocking harder
  Z-height problem, too big transistors, holes in

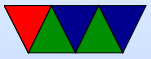


motherboard for capacitors and inductors (for tablets want as flat as possible)



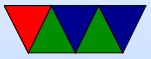
Skylake Processor – Page 4

- New socket, LGA 1151 (soldered use BGA 1515, BGA 1356 and BGA 1440), not back compatible
- Intel RST on PCIe storage?
- USB-A vs USB-C, thunderbolt
- DRAM: DDR3L vs DDR4. SO-DIMM?
- Two memory controllers per channel. Max of 4*16GB = 64GB

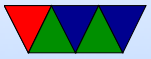


Skylake Processor – Page 5

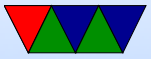
- Performance clock-per-clock only 6% over haswell and 3% over broadwell
- Larger instruction window, extract more parallelism
- Can dispatch 6 uops at once (over 4uops for Haswell)
- “Higher-capacity and improved” branch predictor
- “Faster prefetch”



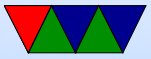
- Shorter latencies
- more units
- Power down when not in use
- Speedup AES-GCM and AES-CBC
- Improved Divider
- FMultiplier regress to Haswell numbers because it allows better performance for enterprise silicon?
- FMUL only disclosed when asked about a rumor?



- Deeper store buffer
- Improved page miss handling (probably mem not tlb?)
- Better L2 cache miss bandwidth
- New instructions for cache management (for NVRAM?)
- Better hyperthreading
- L2 reduced from 8-way to 4-way. Saves power and area? Similar to Haswell performance with lower power

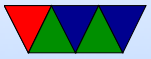


- Intel sells custom configured silicon if you are a bit enough customer
- Security Tech – SGX software guard extensions? Encrypted memory (why is that a good idea?)
- Intel MPX (memory stack/heap protection)
- Trusted execution, protected enclaves
- eDRAM – embedded DRAM – L4 cache? Gor graphics card? 64MB and 128MB



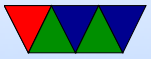
Skylake Processor – Page 6

- Graphics
- Multiple graphics sizes, can scale for power on smaller
- Losless data compression – save power and perf by compressing before sending across bus
- 16-bit float support – less accuracy, lower power
- MPO – multiplane overlay



Skylake Processor – Page 7

- Speed shift
- System Agent
- PCU – power control unit, possibly even embedded intel CPU RAPL?
- Up to 4 independent power domains
- High granularity power gating, at least 12 gates

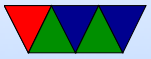


- Several frequency domains: core, uncore, 2 GPU, eDRAM

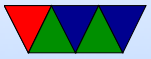
- Intel Speed Shift – let CPU control power, rather than the OS. OS can take up to 30ms to adjust, chip can do it in 1ms.

- HAVE CMOS power equation, but say dynamic plus static is approximagely f**3

- Psys, knows total system power total power provided to CPU



- Race to Idle
- Diminishing returns. Reintroduce idea of duty cycle (see old p4 implementation)
- Can turn off CPU cores as often as 800us



Skylake Processor – Page 8

- Kaby Lake (kah-bee lake)