ECE571: Advanced Microprocessor Design – Homework 9
Fall 2019

Due: Thursday 14 November 2019, 2:00pm

Create a document that contains the answers to the questions below. A .pdf or .txt file is preferred but I can accept MS Office or Libreoffice format if necessary.

1. Read the website article:

   AMD Zen 2 Microarchitecture Analysis: Ryzen 3000 and EPYC Rome by Ian Cutress (note that there are 12 pages to this article).

   `https://www.anandtech.com/show/14525/amd-zen-2-microarchitecture-analysis-ryzen-3000-and-epyc-rome`

   I apologize for the obnoxious ads while reading. Pressing "print this article" and reading that might help make it a bit more readable.

2. Answer the following questions:

   (a) What is a chiplet?

   (b) How quickly is Zen2 able to change frequencies when frequency scaling?

   (c) What is the new CLWB instruction used for?

   (d) What type of branch predictor does Zen2 use?

   (e) Why did AMD reduce the size of the L1 instruction cache?

3. **Submitting your work.**

   - Create the document containing the answers to the questions asked.
   - Please make sure your name appears in the document.
   - e-mail the file to me by the homework deadline.