The following is copied from "STM32L15xxx reference manual (RM0038)."

RCC Register Map

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	**RCC_CR**	Reserved	RTCPRE1	RTCPRE0	CSSON	Reserved		PLL RDY	PLL ON	Reserved					HSEBYP	HSERDY	HSEON	Reserved						MSIRDY	MSION	Reserved							HSIRDY	HSION
	Reset value		0	0	0			0	0						0	0	0							1	1								0	0
0x04	**RCC_ICSCR**	MSITRIM[7:0]								MSICAL[7:0]								MSIRANGE[2:0]			HSITRIM[4:0]					HSICAL[7:0]							
	Reset value	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x	1	0	1	1	0	0	0	0	x	x	x	x	x	x	x	x
0x08	**RCC_CFGR**	Reserved	MCOPRE [2:0]			Reserved	MCOSEL [2:0]			PLL DIV [1:0]		PLLMUL[3:0]				Reserved	PLLSRC	Reserved		PPRE2 [2:0]			PPRE1 [2:0]			HPRE[3:0]				SWS [1:0]		SW [1:0]	
	Reset value		0	0	0		0	0	0	0	0	0	0	0	0		0			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0C	**RCC_CIR**	Reserved								CSSC	LSECSSC	MSIRDYC	PLLRDYC	HSERDYC	HSIRDYC	LSERDYC	LSIRDYC	Reserved	LSECSSIE	MSIRDYIE	PLLRDYIE	HSERDYIE	HSIRDYIE	LSERDYIE	LSIRDYIE	CSSF	Reserved	MSIRDYF	PLLRDYF	HSERDYF	HSIRDYF	LSERDYF	LSIRDYF
	Reset value									0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0		0	0	0	0	0	0
0x10	**RCC_AHBRSTR**	Reserved	FSMCRST	Reserved		AESRST	Reserved	DMA2RST	DMA1RST	Reserved								FLITFRST	Reserved		CRCRST	Reserved				GPIOGRST	GPIOFRST	GPIOHRST	GPIOERST	GPIODRST	GPIOCRST	GPIOBRST	GPIOARST
	Reset value		0					0	0									0			0					0	0	0	0	0	0	0	0
0x14	**RCC_APB2RSTR**	Reserved																	USART1RST	Reserved	SPI1RST	SDIORST	Reserved	ADC1RST	Reserved				TM11RST	TM10RST	TIM9RST	Reserved	SYSCFGRST
	Reset value																		0		0	0		0					0	0	0		0
0x18	**RCC_APB1RSTR**	COMPRST	Reserved	DACRST	PWRRST	Reserved				USBRST	I2C2RST	I2C1RST	UART5RST	UART4RST	USART3RST	USART2RST	Reserved	SPI3RST	SPI2RST	Reserved	WWDRST	Reserved	LCDRST	Reserved			TIM7RST	TIM6RST	TIM5RST	TIM4RST	TIM3RST	TIM2RST
	Reset value	0		0	0					0	0	0	0	0	0	0		0	0		0		0				0	0	0	0	0	0
0x1C	**RCC_AHBENR**	Reserved	FSMCEN	Reserved		AESEN	Reserved	DMA2EN	DMA1EN	Reserved								FLITFEN	Reserved		CRCEN	Reserved				GPIOPGEN	GPIOPFEN	GPIOPHEN	GPIOPEEN	GPIOPDEN	GPIOPCEN	GPIOPBEN	GPIOPAEN
	Reset value		0			0		0	0									1			0					0	0	0	0	0	0	0	0
0x20	**RCC_APB2ENR**	Reserved																	USART1EN	Reserved	SPI1EN	SDIOEN	Reserved	ADC1EN	Reserved				TIM11EN	TIM10EN	TIM9EN	Reserved	SYSCFGEN
	Reset value																		0		0	0		0					0	0	0		0
0x24	**RCC_APB1ENR**	COMPEN	Reserved	DACEN	PWREN	Reserved				USBEN	I2C2EN	I2C1EN	USART5EN	USART4EN	USART3EN	USART2EN	Reserved	SPI3EN	SPI2EN	Reserved	WWDGEN	Reserved	LCDEN	Reserved			TIM7EN	TIM6EN	TIM5EN	TIM4EN	TIM3EN	TIM2EN
	Reset value	0		0	0					0	0	0	0	0	0	0		0	0		0		0				0	0	0	0	0	0
0x28	**RCC_AHBLP ENR**	Reserved	FSMCLPEN	Reserved		AESLPEN	Reserved	DMA2LPEN	DMA1LPEN	Reserved								SRAMLPEN	FLITFLPEN	Reserved	CRCLPEN	Reserved				GPIOGLPEN	GPIOFLPEN	GPIOHLPEN	GPIOELPEN	GPIODLPEN	GPIOCLPEN	GPIOBLPEN	GPIOALPEN
	Reset value		1			1		1	1									1	1		1					1	1	1	1	1	1	1	1
0x2C	**RCC_APB2LP ENR**	Reserved																	USART1LPEN	Reserved	SPI1LPEN	SDIOLPEN	Reserved	ADC1LPEN	Reserved				TIM11LPEN	TIM10LPEN	TIM9LPEN	Reserved	SYSCFGLPEN
	Reset value																		1		1	1		1					1	1	1		1

0x30	**RCC_APB1LPENR**	COMPLPEN	Reserved	DACLPEN	PWRLPEN	Reserved				USBLPEN	I2C2LPEN	I2C1LPEN	USART5LPEN	USART4LPEN	USART3LPEN	USART2LPEN	Reserved	SPI3LPEN	SPI2LPEN	Reserved		WWDGLPEN	Reserved	LCDLPEN	Reserved			TIM7LPEN	TIM6LPEN	TIM5LPEN	TIM4LPEN	TIM3LPEN	TIM2LPEN
	Reset value	1		1	1					1	1	1	1	1	1	1		1	1			1		1				1	1	1	1	1	1
0x034	**RCC_CSR**	LPWRSTF	WWDGRSTF	IWDGRSTF	SFTRSTF	PORRSTF	PINRSTF	OBLRSTF	RMVF	RTCRST	RTCEN	Reserved					RTC SEL [1:0]		Reserved			LSECSSD	LSECSSON	LSEBYP	LSERDY	LSEON	Reserved					LSIRDY	LSION
	Reset value	0	0	0	0	1	1	0	0	0	0						0	0				0	0	0	0						0	0

5.3.1 Clock control register (RCC_CR)

Address offset: 0x00

Reset value: 0x0000 0300

Access: no wait state, word, half-word and byte access

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	RTCPRE[1:0]		CSS ON	Reserved		PLL RDY	PLLON	Reserved					HSE BYP	HSE RDY	HSE ON
	rw	rw	rw			r	rw						rw	r	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						MSI RDY	MSION	Reserved						HSI RDY	HSION
						r	rw							r	rw

Bit 31 Reserved, must be kept at reset value.

Bits 30:29 **RTCPRE[1:0]** RTC/LCD prescaler

These bits are set and reset by software to obtain a 1 MHz clock from HSE. This prescaler cannot be modified if HSE is enabled (HSEON = 1).

00: HSE is divided by 2 for RTC/LCD clock

01: HSE is divided by 4 for RTC/LCD clock

10: HSE is divided by 8 for RTC/LCD clock

11: HSE is divided by 16 for RTC/LCD clock

Bit 28 **CSSON**: Clock security system enable

This bit is set and cleared by software to enable the clock security system (CSS). When CSSON is set, the clock detector is enabled by hardware when the HSE oscillator is ready, and disabled by hardware if an oscillator failure is detected.

0: Clock security system OFF (clock detector OFF)

1: Clock security system ON (clock detector ON if HSE oscillator is stable, OFF otherwise) Bit 27:26

Reserved, must be kept at reset value.

Bit 25 **PLLRDY:** PLL clock ready flag

This bit is set by hardware to indicate that the PLL is locked.

0: PLL unlocked

1: PLL locked

Bit 24 **PLLON:** PLL enable

This bit is set and cleared by software to enable PLL.

Cleared by hardware when entering Stop or Standby mode. This bit can not be reset if the PLL clock is used as system clock or is selected to become the system clock.

0: PLL OFF

1: PLL ON

Bits 23:19 Reserved, must be kept at reset value.

Bit 18 **HSEBYP**: HSE clock bypass

This bit is set and cleared by software to bypass the oscillator with an external clock. The external clock must be enabled with the HSEON bit, to be used by the device.
The HSEBYP bit can be written only if the HSE oscillator is disabled.
0: HSE oscillator not bypassed
1: HSE oscillator bypassed with an external clock

Bit 17 **HSERDY**: HSE clock ready flag

This bit is set by hardware to indicate that the HSE oscillator is stable. After the HSEON bit is cleared, HSERDY goes low after 6 HSE oscillator clock cycles.
0: HSE oscillator not ready
1: HSE oscillator ready

Bit 16 **HSEON**: HSE clock enable

This bit is set and cleared by software.
Cleared by hardware to stop the HSE oscillator when entering Stop or Standby mode. This bit cannot be reset if the HSE oscillator is used directly or indirectly as the system clock.
0: HSE oscillator OFF
1: HSE oscillator ON

Bits 15:10 Reserved, must be kept at reset value.

Bit 9 **MSIRDY**: MSI clock ready flag

This bit is set by hardware to indicate that the MSI oscillator is stable.
0: MSI oscillator not ready
1: MSI oscillator ready

Note: Once the MSION bit is cleared, MSIRDY goes low after 6 MSI clock cycles.

Bit 8 **MSION**: MSI clock enable

This bit is set and cleared by software.
Set by hardware to force the MSI oscillator ON when exiting from Stop or Standby mode, or in case of a failure of the HSE oscillator used directly or indirectly as system clock. This bit cannot be cleared if the MSI is used as system clock.
0: MSI oscillator OFF
1: MSI oscillator ON

Bits 7:2 Reserved, must be kept at reset value.

Bit 1 **HSIRDY**: Internal high-speed clock ready flag

This bit is set by hardware to indicate that the HSI oscillator is stable. After the HSION bit is cleared, HSIRDY goes low after 6 HSI clock cycles.
0: HSI oscillator not ready
1: HSI oscillator ready

Bit 0 **HSION**: Internal high-speed clock enable

This bit is set and cleared by software.
This bit cannot be cleared if the HSI is used directly or indirectly as the system clock.
0: HSI oscillator OFF
1: HSI oscillator ON

5.3.2 Internal clock sources calibration register (RCC_ICSCR)

Address offset: 0x04

Reset value: 0x00XX B0XX where X is undefined. Access: no

wait state, word, half-word and byte access

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSITRIM[7:0]								MSICAL[7:0]							
rw	rw	rw	rw	rw	rw	rw	rw	r	r	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSIRANGE[2:0]			HSITRIM[4:0]					HSICAL[7:0]							
rw	rw	rw	rw	rw	rw	rw	rw	r	r	r	r	r	r	r	r

Bits 31:24 **MSITRIM[7:0]**: MSI clock trimming

These bits are set by software to adjust MSI calibration.

These bits provide an additional user-programmable trimming value that is added to the MSICAL[7:0] bits. They can be programmed to compensate for the variations in voltage and temperature that influence the frequency of the internal MSI RC.

Bits 23:16 **MSICAL[7:0]**: MSI clock calibration

These bits are automatically initialized at startup.

Bits 15:13 **MSIRANGE[2:0]**: MSI clock ranges

These bits are set by software to choose the frequency range of MSI.7 frequency ranges are available:
000: range 0 around 65.536 kHz
001: range 1 around 131.072 kHz
010: range 2 around 262.144 kHz
011: range 3 around 524.288 kHz
100: range 4 around 1.048 MHz
101: range 5 around 2.097 MHz (reset value)
110: range 6 around 4.194 MHz
111: not allowed

Bits 12:8 **HSITRIM[4:0]**: High speed internal clock trimming

These bits provide an additional user-programmable trimming value that is added to the HSICAL[7:0] bits. They can be programmed to compensated for the variations in voltage and temperature that influence the frequency of the internal HSI RC.

Bits 7:0 **HSICAL[7:0]** Internal high speed clock calibration

These bits are initialized automatically at startup.

5.3.3 Clock configuration register (RCC_CFGR)

Address offset: 0x08

Reset value: 0x0000 0000

Access: 0 ≤ wait state ≤ 2, word, half-word and byte access

1 or 2 wait states inserted only if the access occurs during clock source switch.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	MCOPRE[2:0]			Res.	MCOSEL[2:0]			PLLDIV[1:0]		PLLMUL[3:0]				Res.	PLL SRC
	rw	rw	rw		rw	rw	rw	rw	rw	rw	rw	rw	rw		rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	PPRE2[2:0]			PPRE1[2:0]			HPRE[3:0]				SWS[1:0]		SW[1:0]		
	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	r	r	rw	rw	

Bits 31 Reserved, must be kept at reset value.

Bits 30:28 **MCOPRE[2:0]:** Microcontroller clock output prescaler

These bits are set and cleared by software.

It is highly recommended to change this prescaler before MCO output is enabled.

000: MCO is divided by 1
001: MCO is divided by 2
010: MCO is divided by 4
011: MCO is divided by 8
100: MCO is divided by 16
Others: not allowed

Bits 27 Reserved, must be kept at reset value.

Bits 26:24 **MCOSEL[2:0]:** Microcontroller clock output selection

These bits are set and cleared by software.
000: MCO output disabled, no clock on MCO
001: SYSCLK clock selected
010: HSI oscillator clock selected
011: MSI oscillator clock selected
100: HSE oscillator clock selected
101: PLL clock selected
110: LSI oscillator clock selected
111:LSE oscillator clock selected

Note: This clock output may have some truncated cycles at startup or during MCO clock source switching.

Bits 23:22 **PLLDIV[1:0]**: PLL output division

These bits are set and cleared by software to control PLL output clock division from PLL VCO clock. These bits can be written only when the PLL is disabled.
00: not allowed
01: PLL clock output = PLLVCO / 2
10: PLL clock output = PLLVCO / 3
11: PLL clock output = PLLVCO / 4

Bits 21:18 **PLLMUL[3:0]:** PLL multiplication factor

These bits are written by software to define the PLL multiplication factor to generate the PLL VCO clock. These bits can be written only when the PLL is disabled.
0000: PLLVCO = PLL clock entry x 3
0001: PLLVCO = PLL clock entry x 4
0010: PLLVCO = PLL clock entry x 6
0011: PLLVCO = PLL clock entry x 8
0100: PLLVCO = PLL clock entry x 12
0101: PLLVCO = PLL clock entry x 16
0110: PLLVCO = PLL clock entry x 24
0111: PLLVCO = PLL clock entry x 32
1000: PLLVCO = PLL clock entry x 48 others:
not allowed

Caution: The PLL VCO clock frequency must not exceed 96 MHz when the product is in Range 1, 48 MHz when the product is in Range 2 and 24 MHz when the product is in Range 3.

Bit 17 Reserved, must be kept at reset value. Bit 16

PLLSRC: PLL entry clock source

This bit is set and cleared by software to select PLL clock source. This bit can be written only when PLL is disabled.
0: HSI oscillator clock selected as PLL input clock
1: HSE oscillator clock selected as PLL input clock

Note: The PLL minimum input clock frequency is 2 MHz.

Bits 15:14 Reserved, must be kept at reset value.

Bits 13:11 **PPRE2[2:0]**: APB high-speed prescaler (APB2)

These bits are set and cleared by software to control the division factor of the APB high- speed clock (PCLK2).
0xx: HCLK not divided

100: HCLK divided by 2
101: HCLK divided by 4
110: HCLK divided by 8
111: HCLK divided by 16

Bits 10:8 **PPRE1[2:0]**: APB low-speed prescaler (APB1)

These bits are set and cleared by software to control the division factor of the APB low- speed clock (PCLK1).

0xx: HCLK not divided
100: HCLK divided by 2
101: HCLK divided by 4
110: HCLK divided by 8
111: HCLK divided by 16

Bits 7:4 **HPRE[3:0]:** AHB prescaler

These bits are set and cleared by software to control the division factor of the AHB clock.

Caution: Depending on the device voltage range, the software has to set correctly these bits to ensure that the system frequency does not exceed the maximum allowed frequency (for more details please refer to the Dynamic voltage scaling management section in the PWR chapter.) After a write operation to these bits and before decreasing the voltage range, this register must be read to be sure that the new value has been taken into account.

0xxx: SYSCLK not divided
1000: SYSCLK divided by 2
1001: SYSCLK divided by 4
1010: SYSCLK divided by 8
1011: SYSCLK divided by 16
1100: SYSCLK divided by 64
1101: SYSCLK divided by 128
1110: SYSCLK divided by 256
1111: SYSCLK divided by 512

Bits 3:2 **SWS[1:0]**: System clock switch status

These bits are set and cleared by hardware to indicate which clock source is used as system clock.

00: MSI oscillator used as system clock
01: HSI oscillator used as system clock
10: HSE oscillator used as system clock
11: PLL used as system clock

Bits 1:0 **SW[1:0]**: System clock switch

These bits are set and cleared by software to select SYSCLK source.

Set by hardware to force MSI selection when leaving Stop and Standby mode or in case of failure of the HSE oscillator used directly or indirectly as system clock (if the Clock Security System is enabled).

00: MSI oscillator used as system clock
01: HSI oscillator used as system clock
10: HSE oscillator used as system clock
11: PLL used as system clock

5.3.4 Clock interrupt register (RCC_CIR)

Address offset: 0x0C Reset value:

0x0000 0000

Access: no wait state, word, half-word and byte access

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								CSSC	LSECSSC	MSIRDYC	PLLRDYC	HSERDYC	HSIRDYC	LSERDYC	LSIRDYC
								w	w	w	w	w	w	w	w
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res.	LSECSSIE	MSIRDYIE	PLLRDYIE	HSERDYIE	HSIRDYIE	LSERDYIE	LSIRDYIE	CSSF	LSECSSF	MSIRDYF	PLLRDYF	HSERDYF	HSIRDYF	LSERDYF	LSIRDYF
	rw	rw	rw	rw	rw	rw	rw	r	r	r	r	r	r	r	r

Bits 31:24 Reserved, must be kept at reset value.

Bit 23 **CSSC:** Clock security system interrupt clear

This bit is set by software to clear the CSSF flag.

0: No effect

1: Clear CSSF flag

Bit 22 **LSECSSC:** LSE CSS interrupt clear

Set by software to clear LSECSSF. Reset by hardware when clear done.

0: LSECSSF not cleared

1: LSECSSF cleared

Note: This bit is available in high and medium+ density devices only.

Bit 21 **MSIRDYC:** MSI ready interrupt clear

This bit is set by software to clear the MSIRDYF flag.

0: No effect

1: MSIRDYF cleared

Bit 20 **PLLRDYC:** PLL ready interrupt clear

This bit is set by software to clear the PLLRDYF flag.

0: No effect

1: PLLRDYF cleared

Bit 19 **HSERDYC:** HSE ready interrupt clear

This bit is set by software to clear the HSERDYF flag.

0: No effect

1: HSERDYF cleared

Bit 18 **HSIRDYC:** HSI ready interrupt clear

This bit is set software to clear the HSIRDYF flag.

0: No effect

1: HSIRDYF cleared

Bit 17 **LSERDYC:** LSE ready interrupt clear

This bit is set by software to clear the LSERDYF flag.

0: No effect

1: LSERDYF cleared

Bit 16 **LSIRDYC:** LSI ready interrupt clear

This bit is set by software to clear the LSIRDYF flag.

0: No effect

1: LSIRDYF cleared

Bit 15 Reserved, must be kept at reset value. Bit 14

LSECSSIE: LSE CSS interrupt enable

Set and reset by software to enable/disable interrupts from the Clock Security System on external 32 kHz oscillator (LSE).

0: LSE CSS interrupt disabled

1: LSE CSS interrupt enabled

Note: This bit is available in high and medium+ density devices only.

Bit 13 **MSIRDYIE:** MSI ready interrupt enable

This bit is set and cleared by software to enable/disable interrupt caused by the MSI oscillator stabilization.

0: MSI ready interrupt disabled

1: MSI ready interrupt enabled

Bit 12 **PLLRDYIE:** PLL ready interrupt enable

This bit is set and cleared by software to enable/disable interrupt caused by PLL lock.

0: PLL lock interrupt disabled

1: PLL lock interrupt enabled

Bit 11 **HSERDYIE:** HSE ready interrupt enable

This bit is set and cleared by software to enable/disable interrupt caused by the HSE oscillator stabilization.

0: HSE ready interrupt disabled

1: HSE ready interrupt enabled

Bit 10 **HSIRDYIE:** HSI ready interrupt enable

This bit is set and cleared by software to enable/disable interrupt caused by the HSI oscillator stabilization.

0: HSI ready interrupt disabled

1: HSI ready interrupt enabled

Bit 9 **LSERDYIE:** LSE ready interrupt enable

This bit is set and cleared by software to enable/disable interrupt caused by the LSE oscillator stabilization.

0: LSE ready interrupt disabled

1: LSE ready interrupt enabled

Bit 8 **LSIRDYIE:** LSI ready interrupt enable

This bit is set and cleared by software to enable/disable interrupt caused by LSI oscillator stabilization.

0: LSI ready interrupt disabled

1: LSI ready interrupt enabled

Bit 7 **CSSF:** Clock security system interrupt flag

This bit is set by hardware when a failure is detected in the HSE oscillator. It is cleared by software by setting the CSSC bit.

0: No clock security interrupt caused by HSE clock failure

1: Clock security interrupt caused by HSE clock failure

Bit 6 **LSECSSF** LSE CSS Interrupt flag

Reset by software by writing to the LSECSSC bit. Set by hardware when a failure is detected on the external 32 KHz oscillator and the LSECSSIE bit is set.

0: No failure detected on the external 32 KHz oscillator (LSE)

1: A failure is detected on the external 32 kHz oscillator (LSE)

Note: This bit is available in high and medium+ density devices only.

Bit 5 **MSIRDYF:** MSI ready interrupt flag

This bit is set by hardware when the MSI becomes stable and MSIRDYDIE is set. It is cleared by software setting the MSIRDYC bit.

0: No clock ready interrupt caused by the MSI

1: Clock ready interrupt caused by the MSI

Bit 4 **PLLRDYF:** PLL ready interrupt flag

This bit is set by hardware when the PLL locks and PLLRDYDIE is set. It is cleared by software setting the PLLRDYC bit.

0: No clock ready interrupt caused by PLL lock

1: Clock ready interrupt caused by PLL lock

Bit3 **HSERDYF:** HSE ready interrupt flag
This bit is set by hardware when HSE becomes stable and HSERDYDIE is set. It is cleared by software setting the HSERDYC bit.
0: No clock ready interrupt caused by the HSE
1: Clock ready interrupt caused by the HSE

Bit 2 **HSIRDYF:** HSI ready interrupt flag
This bit is set by hardware when the HSI becomes stable and HSIRDYDIE is set. It is cleared by software setting the HSIRDYC bit.
0: No clock ready interrupt caused by the HSI
1: Clock ready interrupt caused by the HSI

Bit 1 **LSERDYF:** LSE ready interrupt flag
This bit is set by hardware when the LSE becomes stable and LSERDYDIE is set. It is cleared by software setting the LSERDYC bit.
0: No clock ready interrupt caused by the LSE
1: Clock ready interrupt caused by the LSE

Bit 0 **LSIRDYF:** LSI ready interrupt flag
This bit is set by hardware when the LSI becomes stable and LSIRDYDIE is set. It is cleared by software setting the LSIRDYC bit.
0: No clock ready interrupt caused by the LSI
1: Clock ready interrupt caused by the LSI

5.3.5 AHB peripheral reset register (RCC_AHBRSTR)

Address offset: 0x10

Reset value: 0x0000 0000

Access: no wait state, word, half-word and byte access.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	FSMC RST	Reserved		AES RST	Res.	DMA2RST	DMA1RST	Reserved							
	rw			rw		rw	rw								

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FLITF RST	Reserved		CRC RST	Reserved				GPIOG RST	GPIOF RST	GPIOH RST	GPIOE RST	GPIOD RST	GPIOC RST	GPIOB RST	GPIOA RST
rw			rw					rw	rw	rw	rw	rw	rw	rw	rw

Bit 31 Reserved, must be kept at reset value.

Bit 30 **FSMCRST:** FSMC reset
This bit is set and cleared by software.
0: No effect
1: Reset FSMC
Note: This bit is available in high density devices only.

Bits 29:28 Reserved, must be kept at reset value

Bit 27 **AESRST:** AES reset
This bit is set and cleared by software.
0: No effect
1: Reset AES
Note: This bit is available in STM32L16x devices only.

Bit 26 Reserved, must be kept at reset value. Bit 25

DMA2RST: DMA2 reset

This bit is set and cleared by software.

0: No effect

1: Reset DMA2

Note: This bit is available in high and medium+ density devices only.

Bit 24 **DMA1RST:** DMA1 reset

This bit is set and cleared by software.

0: No effect

1: Reset DMA1

Bits 23:16 Reserved, must be kept at reset value.

Bit 15 **FLITFRST:** FLITF reset

This bit is set and cleared by software. The FLITF reset can be enabled only when the Flash memory is in power down mode.

0: No effect

1: Reset FLITF

Bits 14:13 Reserved, must be kept at reset value.

Bit 12 **CRCRST:** CRC reset

This bit is set and cleared by software.

0: No effect

1: Reset CRC

Bits 11:8 Reserved, must be kept at reset value.

Bit 7 **GPIOGRST:** IO port G reset

This bit is set and cleared by software.

0: No effect

1: Reset IO port G

Note: This bit is available in high and medium+ density devices only.

Bit 6 **GPIOFRST:** IO port F reset

This bit is set and cleared by software.

0: No effect

1: Reset IO port F

Note: This bit is available in high and medium+ density devices only.

Bit 5 **GPIOHRST:** IO port H reset

This bit is set and cleared by software.

0: No effect

1: Reset

Bit 4 **GPIOERST:** IO port E reset

This bit is set and cleared by software.

0: No effect

1: Reset IO port E

Bit 3 **GPIODRST:** IO port D reset

This bit is set and cleared by software.

0: No effect

1: Reset IO port D

Bit 2 **GPIOCRST:** IO port C reset

This bit is set and cleared by software.

0: No effect

1: Reset IO port C

Bit 1 **GPIOBRST:** IO port B reset
This bit is set and cleared by software.
0: No effect
1: Reset IO port B

Bit 0 **GPIOARST:** IO port A reset
This bit is set and cleared by software.
0: No effect
1: Reset IO port A

5.3.6 APB2 peripheral reset register (RCC_APB2RSTR)

Address offset: 0x14

Reset value: 0x00000 0000

Access: no wait state, word, half-word and byte access

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res.	USART1 RST	Res.	SPI1 RST	SDIO RST	Res.	ADC1 RST	Reserved			TIM11 RST	TIM10 RST	TIM9 RST	Res.	SYSCF GRST	
	rw		rw	rw		rw				rw	rw	rw		rw	

Bits 31:15 Reserved, must be kept at reset value.

Bit 14 **USART1RST:** USART1 reset
This bit is set and cleared by software.
0: No effect
1: Reset USART1

Bit 13 Reserved, must be kept at reset value. Bit 12

SPI1RST: SPI 1 reset
This bit is set and cleared by software.
0: No effect
1: Reset SPI 1

Bit 11 **SDIORST:** SDIO reset
This bit is set and cleared by software.
0: No effect
1: Reset SDIO
Note: This bit is available in high density devices only.

Bit10 Reserved, must be kept at reset value.

Bit 9 **ADC1RST:** ADC1 interface reset
This bit is set and cleared by software.
0: No effect
1: Reset ADC1 interface

Bits 8:5 Reserved, must be kept at reset value.

Bit 4 **TIM11RST:** TIM11 timer reset
Set and cleared by software.
0: No effect
1: Reset TIM11 timer

Bit 3 **TIM10RST:** TIM10 timer reset
This bit is set and cleared by software.

0: No effect
1: Reset TIM10 timer

Bit 2 **TIM9RST:** TIM9 timer reset
This bit is set and cleared by software.
0: No effect
1: Reset TIM9 timer

Bit 1 Reserved, must be kept at reset value.

Bit 0 **SYSCFGRST:** System configuration controller reset
This bit is set and cleared by software.
0: No effect
1: Reset System configuration controller

5.3.7 APB1 peripheral reset register (RCC_APB1RSTR)

Address offset: 0x18

Reset value: 0x0000 0000

Access: no wait state, word, half-word and byte access

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMP RST	Res.	DAC RST	PWR RST	Reserved				USB RST	I2C2 RST	I2C1 RST	UART5 RST	UART4 RST	USART 3 RST	USART 2 RST	Res.
rw		rw	rw					rw	rw	rw	rw	rw	rw	rw	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI3 RST	SPI2 RST	Reserved		WWDG RST	Res.	LCD RST	Reserved			TIM7 RST	TIM6 RST	TIM5 RST	TIM4 RST	TIM3 RST	TIM2 RST
rw	rw			rw		rw				rw	rw	rw	rw	rw	rw

Bit 31 **COMPRST:** COMP interface reset
This bit is set and cleared by software.
0: No effect
1: Reset COMP interface

Bits 30 Reserved, must be kept at reset value. Bit 29

DACRST: DAC interface reset
This bit is set and cleared by software.
0: No effect
1: Reset DAC interface

Bit 28 **PWRRST:** Power interface reset
This bit is set and cleared by software.
0: No effect
1: Reset power interface

Bits 27:24 Reserved, must be kept at reset value.

Bit 23 **USBRST:** USB reset
This bit is set and cleared by software.
0: No effect
1: Reset USB

Bit 22 **I2C2RST:** I^2C 2 reset
This bit is set and cleared by software.
0: No effect
1: Reset I^2C 2

Bit 21 **I2C1RST:** I^2C 1 reset
This bit is set and cleared by software.
0: No effect
1: Reset I^2C 1

Bit 20 **UART5RST:** UART 5 reset
This bit is set and cleared by software.
0: No effect
1: Reset UART 5
Note: This bit is available in high density devices only.

Bit 19 **UART4RST:** UART 4 reset
This bit is set and cleared by software.
0: No effect
1: Reset UART 4
Note: This bit is available in high density devices only.

Bit 18 **USART3RST:** USART 3 reset
This bit is set and cleared by software.
0: No effect
1: Reset USART 3

Bit 17 **USART2RST:** USART 2 reset
This bit is set and cleared by software.
0: No effect
1: Reset USART 2

Bit16 Reserved, must be kept at reset value. Bit 15

SPI3RST: SPI 3 reset
This bit is set and cleared by software.
0: No effect
1: Reset SPI 3
Note: This bit is available in high and medium+ density devices only.

Bit 14 **SPI2RST:** SPI 2 reset
This bit is set and cleared by software.
0: No effect
1: Reset SPI 2

Bits 13:12 Reserved, must be kept at reset value.

Bit 11 **WWDGRST:** Window watchdog reset
This bit is set and cleared by software.
0: No effect
1: Reset window watchdog

Bits 10 Reserved, must be kept at reset value. Bit 9

LCDRST: LCD reset
This bit is set and cleared by software.
0: No effect
1: Reset LCD

Bits 8:6 Reserved, must be kept at reset value.

Bit 5 **TIM7RST:** Timer 7 reset
This bit is set and cleared by software.
0: No effect
1: Reset timer 7

Bit 4 **TIM6RST:** Timer 6reset
Set and cleared by software.
0: No effect
1: Reset timer 6

Bit 3 **TIM5RST:** Timer 5 reset
Set and cleared by software.
0: No effect
1: Reset timer 5
Note: This bit is available in high and medium+ density devices only.

Bit 2 **TIM4RST:** Timer 4 reset
Set and cleared by software.
0: No effect
1: Reset timer 4

Bit 1 **TIM3RST:** Timer 3 reset
Set and cleared by software.
0: No effect
1: Reset timer 3

Bit 0 **TIM2RST:** Timer 2 reset
Set and cleared by software.
0: No effect
1: Reset timer 2

5.3.8 AHB peripheral clock enable register (RCC_AHBENR)

Address offset: 0x1C Reset

value: 0x0000 8000

Access: no wait state, word, half-word and byte access

Note: When the peripheral clock is not active, the peripheral register values may not be readable by software and the returned value is always 0x0.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	FSMCEN	Reserved		AESEN	Res.	DMA2EN	DMA1EN	Reserved							
	rw			rw		rw	rw								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FLITFEN	Reserved		CRCEN	Reserved				GPIOGEN	GPIOFEN	GPIOHEN	GPIOEEN	GPIODEN	GPIOCEN	GPIOBEN	GPIOAEN
rw			rw					rw	rw	rw	rw	rw	rw	rw	rw

Bit 31 Reserved, must be kept at reset value.

Bit 30 **FSMCEN:** FSMC clock enable
This bit is set and cleared by software.
0: FSMC clock disabled
1: FSMC clock enabled
Note: This bit is available in high density devices only.

Bits 29:28 Reserved, must be kept at reset value.

Bit 27 **AESEN:** AES clock enable
This bit is set and cleared by software.
0: AES clock disabled

1: AES clock enabled

Note: This bit is available in STM32L16x devices only.

Bit 26 Reserved, must be kept at reset value. Bit 25

DMA2EN: DMA2 clock enable

This bit is set and cleared by software.
0: DMA2 clock disabled
1: DMA2 clock enabled

Note: This bit is available in high and medium+ density devices only.

Bit 24 **DMA1EN:** DMA1 clock enable

This bit is set and cleared by software.
0: DMA1 clock disabled
1: DMA1 clock enabled

Bits 23:16 Reserved, must be kept at reset value.

Bit 15 **FLITFEN:** FLITF clock enable

This bit can be written only when the Flash memory is in power down mode.
0: FLITF clock disabled
1: FLITF clock enabled

Bits 14:13 Reserved, must be kept at reset value.

Bit 12 **CRCEN:** CRC clock enable

This bit is set and cleared by software.
0: CRC clock disabled
1: CRC clock enabled

Bits 11:6 Reserved, must be kept at reset value.

Bit 7 **GPIOGEN:** IO port G clock enable

This bit is set and cleared by software.
0: IO port G clock disabled
1: IO port G clock enabled

Note: This bit is available in high and medium+ density devices only.

Bit 6 **GPIOFEN:** IO port F clock enable

This bit is set and cleared by software.
0: IO port F clock disabled
1: IO port F clock enabled

Note: This bit is available in high and medium+ density devices only.

Bit 5 **GPIOHEN:** IO port H clock enable

This bit is set and cleared by software.
0: IO port H clock disabled
1: IO port H clock enabled

Bit 4 **GPIOEEN:** IO port E clock enable

This bit is set and cleared by software.
0: IO port E clock disabled
1: IO port E clock enabled

Bit 3 **GPIODEN:** IO port D clock enable

Set and cleared by software.
0: IO port D clock disabled
1: IO port D clock enabled

Bit 2 **GPIOCEN:** IO port C clock enable

This bit is set and cleared by software.
0: IO port C clock disabled
1: IO port C clock enabled

Bit 1 **GPIOBEN:** IO port B clock enable
This bit is set and cleared by software.
0: IO port B clock disabled
1: IO port B clock enabled

Bit 0 **GPIOAEN:** IO port A clock enable
This bit is set and cleared by software.
0: IO port A clock disabled
1: IO port A clock enabled

5.3.9 APB2 peripheral clock enable register (RCC_APB2ENR)

Address: 0x20

Reset value: 0x0000 0000

Access: word, half-word and byte access

No wait states, except if the access occurs while an access to a peripheral in the APB2 domain is on going. In this case, wait states are inserted until the access to APB2 peripheral is finished.

Note: When the peripheral clock is not active, the peripheral register values may not be readable by software and the returned value is always 0x0.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
rw															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res.	USART1 EN	Res.	SPI1 EN	SDIO EN	Res.	ADC1 EN	Reserved			TIM11 EN	TIM10 EN	TIM9 EN	Res.	SYSCF GEN	
	rw		rw	rw		rw				rw	rw	rw		rw	

Bits 31:15 Reserved, must be kept at reset value.

Bit 14 **USART1EN:** USART1 clock enable
This bit is set and cleared by software.
0: USART1 clock disabled
1: USART1 clock enabled

Bit 13 Reserved, must be kept at reset value. Bit 12

SPI1EN: SPI 1 clock enable
This bit is set and cleared by software.
0: SPI 1 clock disabled
1: SPI 1 clock enabled

Bit 11 **SDIOEN:** SDIO clock enable
This bit is set and cleared by software.
0: SDIO clock disabled
1: SDIO clock enabled
Note: This bit is available in high density devices only.

Bit 10 Reserved, must be kept at reset value. Bit 9

ADC1EN: ADC1 interface clock enable
This bit is set and cleared by software.

0: ADC1 interface disabled
1: ADC1 interface clock enabled

Bits 8:5 Reserved, must be kept at reset value.

Bit 4 **TIM11EN:** TIM11 timer clock enable
This bit is set and cleared by software.
0: TIM11 timer clock disabled
1: TIM11 timer clock enabled

Bit 3 **TIM10EN:** TIM10 timer clock enable
This bit is set and cleared by software.
0: TIM10 timer clock disabled
1: TIM10 timer clock enabled

Bit 2 **TIM9EN:** TIM9 timer clock enable
This bit is set and cleared by software.
0: TIM9 timer clock disabled
1: TIM9 timer clock enabled

Bit 1 Reserved, must be kept at reset value.

Bit 0 **SYSCFGEN:** System configuration controller clock enable
This bit is set and cleared by software.
0: System configuration controller clock disabled
1: System configuration controller clock enabled