Number of memory read and write cycles required for various addressing modes. This does not include any extra time required by processor – only memory reads and writes here.

MODE	Instruction	Fetch	Execute	Instruction	Fetch	Execute
INH	INCA	1	0	INX	1	0
IMM	LDAA #7	2	0	LDX #7	3	0
DIR	LDAA $07	2	1	LDX $07	2	2
EXT	LDAA $7000	3	1	LDX $7000	3	2
IND,X	LDAA 7,X	2	1	LDX 7,X	2	2
IND,Y	LDAA 7,Y	3	1	LDX 7,Y	3	2

Make sure you understand each entry. Don’t miss the fact that LDX #7 takes one more cycle to fetch the instruction than does LDAA #7. Why is this?