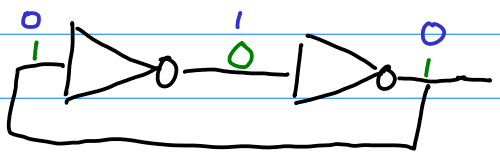
Begin Sequential Logic

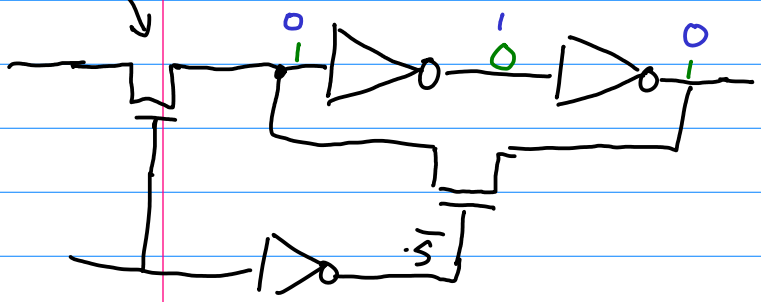
Outputs are a function of present and past inputs
⇒ need memory

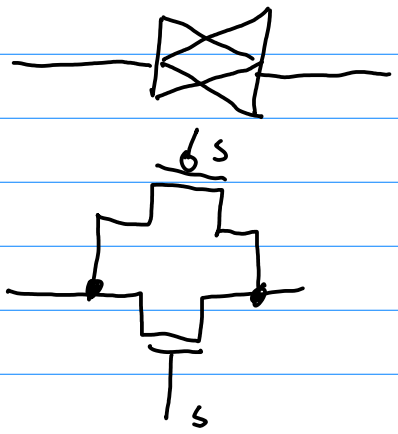
Synchronous Sequential Circuits ← This class
Asynchronous " "

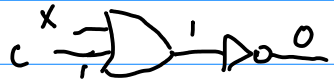


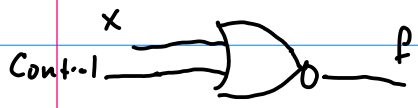
"Bistable"

Transmission Gate



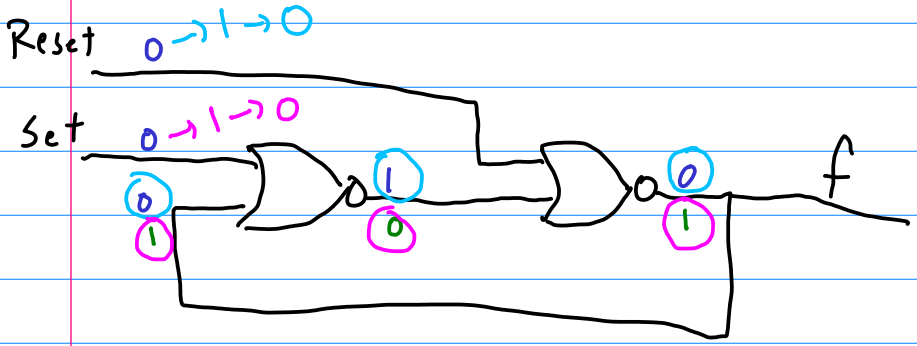






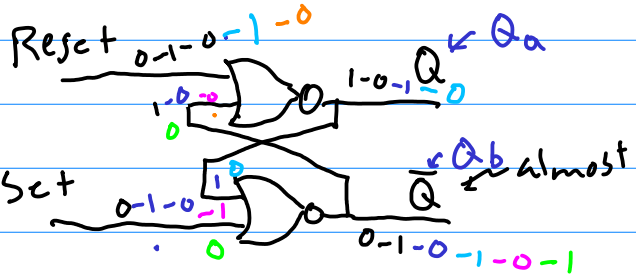
control = 0 $f = \bar{X}$
control = 1 $f = \bar{1} = 0$

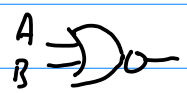
S-R latch



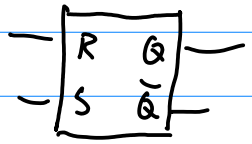
Reset = 1 f → 0
Set = 1 f → 1

Hold state if Reset & Set both 0

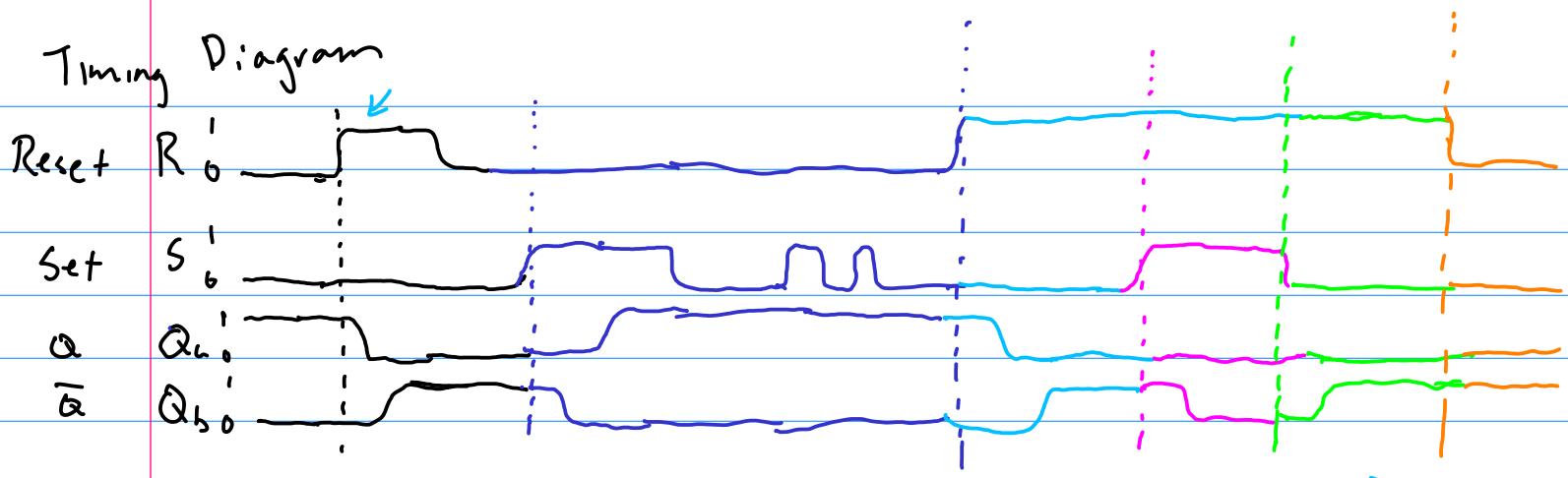




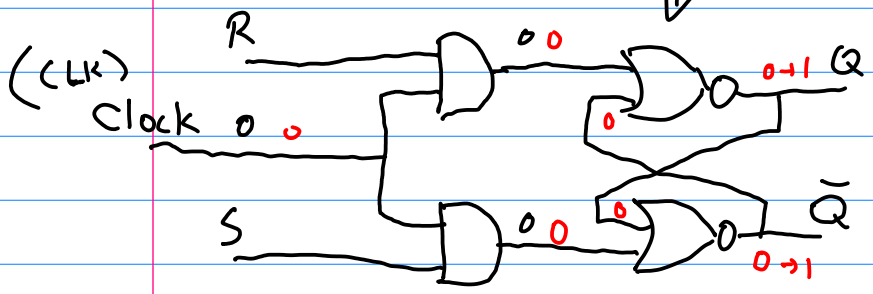
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0



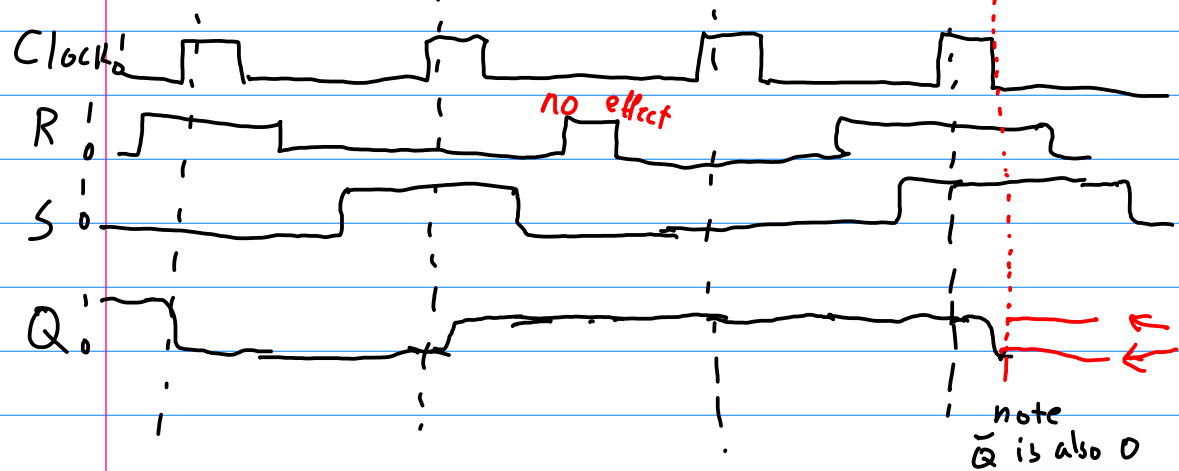
Timing Diagram

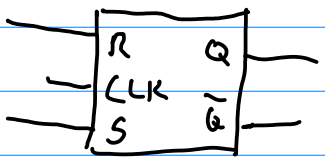


Gated S-R latch

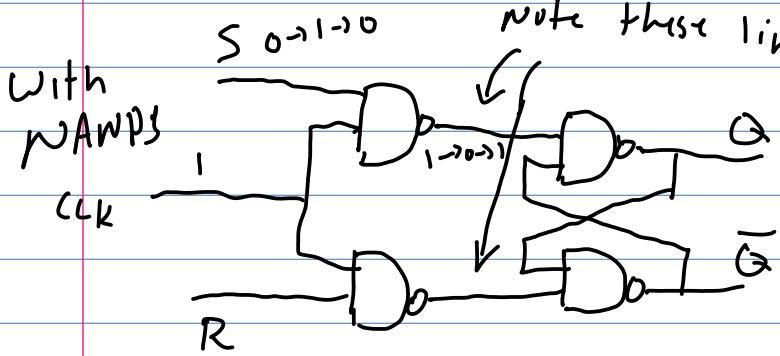


S	R	Q_a (Q)	Q_b ($\bar{Q}$)	
0	0	Q_a	Q_b	no change
0	1	0	1	
1	0	1	0	
1	1	0	0	"illegal"

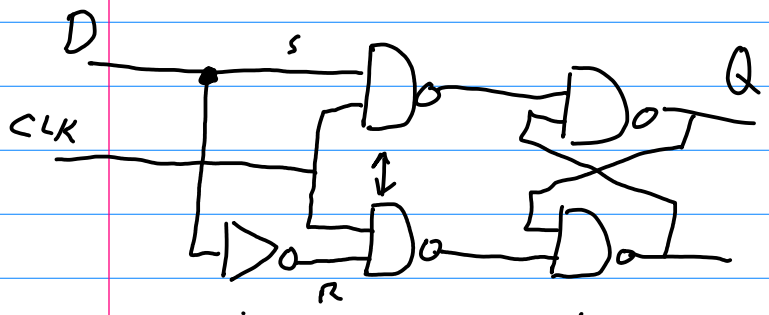




With NANDS



Gated D-latch



CLK	D	Q	
0	X	Q	hold
1	0	0	
1	1	1